1.1.1 and 1.1.2 - Curricular Planning and Implementation

2019-20

PART B

Criterion 1 – Curricular Aspects

Key Indicator – 1.1 Curricular Planning and Implementation

1.1.1 - SUPPORTING DOCUMENTS

FR. Conceicao Rodrigues College of Engineering

1.1.1 Supporting Documents

SAMPLE- CIRCULAR EXECUTIVE COMMITTEE MEETING

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Fr. Agnel Ashram, Bandstand, Bandra (West), Mumbai – 400 050.

Ref.: CRCE / 2019 / 424

Date : October 14, 2019.

NOTICE

To,
The Executive Committee Members

A meeting of the Executive Committee is scheduled on Wednesday, 16th October 2019 at 10.30 AM in the Conference Room (Fifth Floor) to discuss the following matters.

AGENDA

1. Academic Matters
2. Readiness for NAAC Visit

Any other matter with the permission of the Chair.

All the members are requested to attend.

(DR. SRIJA UNNIKRISHNAN)
PRINCIPAL

1. Dr. V.S. Jorapur, HOD – Production Engg.
2. Dr. Sapna Prabhu, HOD – Electronics Engg.
3. Dr. B.S. Daga, HOD – Computer Engg.
4. Dr. Jagruti Save, HOD – Info. Tech.
5. Dr. Hemant Khanolkar, HOD – Hum. & Sci.
6. Dr. S.K. Surve, Dean – Academics
7. Dr. D.V. Bhoir, Dean – Students Affairs
8. Dr. Bhushan Patil, Dean – Research & Development
9. Dr. V.S. Bilolikar, Examination Cell Incharge
8. Mr. Mahesh Sharma, Training & Placement Officer
10. Mr. Chandrashekhar Shetty, Registrar

SAMPLE- MINUTES EXECUTIVE COMMITTEE MEETING

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

Fr. Agnel Ashram, Bandstand, Bandra (W), Mumbai – 400 050.

MINUTES OF THE EXECUTIVE COMMITTEE MEETING HELD ON 20TH JULY 2019 IN THE CONFERENCE ROOM (FIFTH FLOOR) AT 10.00 AM

MEMBERS PRESENT:

1. Dr. Srija Unnikrishnan (In the Chair)
2. Dr. V.S. Jorapur
3. Dr. Sapna Prabhu
4. Dr. B.S. Daga
5. Dr. Jagruti Save
6. Dr. Hemant Khanolkar
7. Dr. D.V. Bhoir
8. Dr. S.K. Surve
9. Dr. Bhushan Patil
10. Mr. Mahesh Sharma

Principal welcomed the members.

Principal briefed members that the main agenda of the meeting is to take follow-up on the agenda items discussed in the previous HODs and Deans meeting held on 29th June 2019.

The following discussions were held:

Item No.1: Project based learning

Principal told members to implement Project based learning at all levels possible – individual subjects, Mini Projects, Dept. wise projects. She said that the objective behind the concept of project based learning it is to engage or get maximum students involved in Projects, thereby enhancing their learning and placement prospects.

Dr. Sapna Prabhu commented that through Project Cell, some projects have been initiated for the E-Yantra competition. Groups of 4 students each from SE & TE classes have been formed and they are assigned the mentors.

Dr. Jagruti Save, informed that many mini-projects are going on in the IT Dept. The third year students are engaged in 4 hours separate project which was started during their second year. Under this project, students have developed 2 modules for website which can facilitate easy data collection. The project is still going on. The problem statement for second Year students is yet to be given. Many students are doing NPTEL courses and internships.

Item No.2: Innovative experiment for each lab. course

For every lab course, each student group can design and implement one innovative experiment, related to the subject. The respective faculty can guide the students. The best innovative experiment subjectwise / yearwise / department wise can be given recognition.

Item No.3: Academic Monitoring

- HODs will follow up the Lesson plan, Tutorial/Practical plan submitted by faculty.

...2/-

- Principal apprised members about the change in FE term commencement date, as the CAP round reporting has been extended. Induction Programme, spread across the year, should be held as specified by the University. Institute should award certificates to all students on successful completion of the Induction Programme, based on their report and presentation. Dr. Hemant Khanolkar read out the schedule of the Induction Programme. Principal told Dr. Khanolkar to prepare an action plan, work out the logistics and keep records of the programmes for issue of certificates.
- Dr. Khanolkar informed that FE Results have been declared and the overall passing percentage of students is 74%. He read out subjectwise and branchwise passing percentages. Student from Production Engg. branch, Mr. Amit Dubey, stood overall first.
- It was decided to hold FE faculty meeting on the coming Monday. Chapter wise notes are to be prepared by faculty for first year students. Hard copy as well as soft copy of the notes can be given to first year students.
- Principal told that faculty members should start doing attendance entries from 19nd July 2019.

Item No.4: Effective use of laboratory slots

- Principal expressed concern that the Lab sessions are not effectively utilised. Placement companies had mentioned about the poor Practical knowledge and experience of students. The tendency of copying/downloading codes/expt. design should be curtailed. Teachers should give multiple and challenging problems to students in the same batch, so that students find solutions on their own. If required, internet can be disabled during specific lab sessions.
- HODs can identify good departmental projects which can be preserved and students re-imbursed, with proper bills. Project competitions can be held department-wise.

There was no other item for discussion.

Principal thanked members for attending the meeting and their active participation.

(Dr. SRIJA UNNIKRISHNAN)
PRINCIPAL

Copy to:

1. Rev. Fr. Peter D'Souza, Local Superior – for information
2. Rev. Fr. Valerian D'Souza, Director – for information
3. Dr. V.S. Jorapur 4. Dr. Sapna Prabhu 5. Dr. B.S. Daga
6. Dr.. Jagruti Save 7. Dr. Hemant Khanolkar 8. Dr. D.V. Bhoir
9. Dr. S.K. Surve 10. Dr. Bhushan Patil 11. Dr. V.S. Bilolikar
12. Mr. Mahesh Sharma 13. Mr. C.B. Shetty

SAMPLE- CIRCULAR DEPARTMENT ADVISORY BOARD MEETING

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Fr. Agnel Ashram, Bandstand, Bandra (west), Mumbai 400050
Department of Computer Engineering

Ref/: CRCE/COMPS/2018_19/DAB/5

Date: 18th June 2019.

CIRCULAR

The Fifth meeting of Departmental Advisory Board(DAB) is scheduled to be held on 26th June 2019 in Computer Lab 6th floor at 10.00AM

Agenda

1. Review of Previous DAB Minutes of Meeting.
2. To get inputs from experts about the actions to be taken with reference to the NBA committee feedback.
3. To discuss the assessment of the attainment of Program Outcomes, Program Specific Outcomes.
4. To discuss about Quality Improvement on academic processes.
5. To establish Centre of Excellence.
6. To promote internship opportunities for students.

Dr B.S. Daga
Head Of the Department,
Department of Computer Engineering,
Fr. Conceicao Rodrigues College of engineering

Members:

1) Dr. Srija Unnikrishnan (Principal, Fr.C.R.C.E.)
2) Dr. B.S.Daga (H.O.D. Computer Dept, Fr.C.R.C.E.)
3) Dr Narendra Shekhokar (Academic Expert, H.O.D. DJS College of Engineering)
4) Ms. Ipsita Bhattacharya (Industry Expert-Business Analyst at JPMorgan Chase & Co., Corporate Social Responsibility Manager at Trishul (NGO), Director of Strategy at Annadhan)
5) Mr. Mohak Gogri (Senior Software Engineer at Mobileum Technologies, Mumbai, Alumni, Fr.C.R.C.E.)
6) Mr. Ruben Monteriao (Software Development Engineer, Media.net, Alumni, Fr.C.R.C.E.)
7) Ms. Meryl Martis(Associate Software Engineer, BNP Paribas ISPL, Alumni, Fr.C.R.C.E.)
8) Prof. Swati Ringe (Program Co-Ordinator, Computer Department, Fr.C.R.C.E)
9) Prof. Sujata Deshmukh (Computer Department, Fr.C.R.C.E.)

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

Fr. Agnel Ashram, Bandstand, Bandra (west), Mumbai 400050
Department of Computer Engineering

Ref/: CRCE/COMPS/2018_19/DAB/5

Date: 26th June 2019.

DAB MEETING ATTENDANCE

The Fifth meeting of Departmental Advisory Board(DAB) is scheduled to be held on 26th June 2019 in Computer Lab 6th floor at 10.00AM.

Agenda

1. Review of Previous DAB Minutes of Meeting.
2. To get inputs from experts about the actions to be taken with reference to the NBA committee feedback.
3. To discuss the assessment of the attainment of Program Outcomes, Program Specific Outcomes.
4. To discuss about Quality Improvement on academic processes.
5. To establish Centre of Excellence.
6. To promote internship opportunities for students.

Members:

1) Dr. Srija Unnikrishnan (Principal, Fr.C.R.C.E.)
2) Dr. B.S.Daga (H.O.D. Computer Dept, Fr.C.R.C.E.)
3) Dr Narendra Shekhokar (Academic Expert, H.O.D. DJS College of Engineering)
4) Ms. Ipsita Bhattacharya (Industry Expert-Business Analyst at JP Morgan Chase & Co., Corporate Social Responsibility Manager at Trishul (NGO), Director of Strategy at Annadhan)
5) Mr. Aditya Desai (Senior Software Engineer at BNP Paribas, Mumbai, Alumni, Fr.C.R.C.E.)
6) Mr. Ruben Monteriao (Software Development Engineer, Media.net, Alumni, Fr.C.R.C.E.)
7) Ms. Meryl Martis(Associate Software Engineer, BNP Paribas ISPL, Alumni, Fr.C.R.C.E.)
8) Prof. Swati Ringe (Program Co-Ordinator, Computer Department, Fr.C.R.C.E)
9) Prof. Sujata Deshmukh (Computer Department, Fr.C.R.C.E.)

SAMPLE- MINUTES DEPARTMENT ADVISORY BOARD MEETING

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering
2019-2020
Minutes of Meeting of DAB

Ref/: CRCE/COMPS/2019_20/DABM/5

Date of meeting: 26th June 2019, Venue: 603 Lab

First Prof. Daga welcomed all the members and discussed the agenda of the meeting . Then he started with presentations. Further he discussed about vision and mission of institute and department. Following are points discussed in the meeting during the presentation of Prof. Daga

Agenda

1. To get inputs from experts about the actions to be taken with reference to the NBA committee feedback.
2. To discuss the assessment of the attainment of Program Outcomes, Program Specific Outcomes.
3. To discuss about Quality Improvement on academic processes.

Discussion and Action:

1) Curriculum gap and Content Beyond syllabus
   - Prof. Daga added that for academic year 18-19, department has communicated the curriculum Gap to BOS chairman, Computer. But there is no proper format from university side.
   - Prof. Shekokar added that there should be credits or marks for value addition courses in aliened with AICTE curriculum.
   - Ms. Ipsita Bhattacharya suggested that alumni can guide about topics for content beyond syllabus which is industry specific.

2) Research paper writing- in discussion following strategies are suggested to improve paper writing for students
   i. Collaborative assignment for paper presentation during Practical session for Second year (project based learning)
   ii. Review paper writing in TE students and one paper on Mini project.
   iii. Paper presentation compulsory for BE projects.

- To motivate students for paper writing – Full paper presentation amount/charges and expenses sponsorship by college.
- Need to create awareness about paper presentation among the students.
- Need of plagiarism checker software for Paper and assignment

3) Consultancy, funded project and Centre of excellence
   - No funded projects because there is no proper dedicated research lab in the department.
   - Motivate the students to do External final year projects- final year projects with industry or company – take problem definition from different companies
   - Target small companies for Final year projects
   - Develop some dedicated labs for consultancy projects according expertise of faculties and market analysis.

4) other issues- suggested by members
   - Need to develop techno-managerial skill in students – leadership skills
   - College to college collaboration to get more exposure to the students
   - College collaboration with IITs or NITs
   - Need to improve college visibility- suggested to involve many companies in fragmag (college magazine and add messages from CEO of different companies. and in this way we can get more sponsorships for the events.
   - Motivate students to add project contents on Github and add the handle in resume, to watch clear coding video
   - Question paper analysis- not/less attempted questions
   - strong students – Harder assignments
   - Internship-
   - Departmental newsletter
   - include case study in subjects

B. S. Daya.

Following members were present in the meeting

Sr. No.	Name of DAB Member	Designation
1	Dr. Narendra Shekokar	H.O.D. Computer Department, D.J. Sanghavi College of Engineering, Mumbai
2	Ms. Ipsita Bhattacharya	Business Analyst at JPMorgan
3	Mr. Mohak Gogri	Senior Software Engineer at Mobileum Technologies
4	Mr. Ruben Monteriao	Software Development Engineer, Media.net
5	Ms. Meryl Martis	Associate Software Engineer, BNP Paribas
6	Dr. B. S. Daga	HOD, Computer engineering, FRCRCE, Bandra
7	Dr. S. K. Surve	Dean Academics, FRCRCE, Bandra
8	Dr. Sujata P. Deshmukh	Program Coordinator, FRCRCE, Bandra
9	Prof. Swati Ringe	PAC committee member, FRCRCE, Bandra

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

Department of Computer Engineering

Form for DAB meeting

Academic Year 2019-20

Date: 26th June 2019 Time: 10:00 am

Venue: Computer Lab 603

Suggestions by DAB Committee Members

1) Suggestion for improvements given by the review of NBA Report

- **PEO, PSO, POs and Cos mapping and attainment need to be well understood by the faculty and applied objectively to improve the teaching – learning.**

Please add your suggestion to improve this point

- CO should be well define by faculty, need to discuss with Industry before starting every chapter. Co-Po Mapping need to Review by domain expert by subject.

- **There is no provision for continuous improvement based on feedback from different stakeholders.**

Please add your suggestion to improve this point

Need to take feedback from Employer (Recruiter).

- **The curriculum gaps need to be identified properly and curriculum difficulties should be brought to the notice of affiliating university.**

Please add your suggestion to improve this point

- curriculum gap need to address by Institute
- Taken good initiative to Communicate curriculum gap to BoS (CS) University of Mumbai

- **There is not much happening beyond syllabus.**

Please add your suggestion to improve this point. Please Give the name of subject and advanced topics for it.

- Motivate student to Enroll more to Course Era & NPTEL Courses.

➢ **Publication in reputed journal publication-**

Pl add your suggestion to improve this point

➢ **Industry-Institute interaction is mostly limited to expert talks. It should be improved to have hands-on experience and working on live projects.**

Pl add your suggestion to improve this point

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2) Suggestion for Center of excellence

1) Please suggest the area for Center of excellence

---

2) Please suggest the Hardware and software configuration for suggested Center of excellence

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- For ML, GPU base H/W is required.

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3) New labs suggestions collaborate with Industries like TCS, Infosys or IIT for new Lab setup.

4) Please suggest the industries for Industrial visit.

During Industries visit student should get opportunities to learn S/W dev. life cycle.

5) Other Suggestions.

- Need to improve Internship.

Name of DAB member : Dr. Narendra M. Thellokar

Sign : Dt: 26/05/2017

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

Department of Computer Engineering

Form for DAB meeting

Academic Year 2019-20

Time: 10:00 am

Date: 26th June 2019

Venue: Computer Lab 603

Suggestions by DAB Committee Members

1) Suggestion for improvements given by the review of NBA Report

- **PEO, PSO, POs and Cos mapping and attainment need to be well understood by the faculty and applied objectively to improve the teaching – learning.**

Please add your suggestion to improve this point
- Have an idea of how concepts can be used in real life challenge statements.
- Be a part of LinkedIn ambassador programs where students will get exposure
- students to participate in Hackathons/ coding competitions

- **There is no provision for continuous improvement based on feedback from different stakeholders.**

Please add your suggestion to improve this point
Have a dedicated group of Board members from corporate preferably college alumni to keep meeting department head & design a curriculum that should help students to bridge the gap.

- **The curriculum gaps need to be identified properly and curriculum difficulties should be brought to the notice of affiliating university.**

Please add your suggestion to improve this point
Take up some online courses from courseras (for example: Machine learning by standford university) These really help to improve knowledge and make students industry ready. apart from having industry ready certificates

- **There is not much happening beyond syllabus.**

Please add your suggestion to improve this point. Please Give the name of subject and advanced topics for it.

1) Invite lecturers from IIT for 2 to 3 days courses
2) Encourage industry experts to talk about upcoming buzzing topics and train students
3) conduct certification course workshops over the semester break for interested students (eg. Python)
4) Introduce concepts like Agile Software Development model as industry thrives on it

➢ **Publication in reputed journal publication-**

PI add your suggestion to improve this point → 1) Maintain profiles on LinkedIn & Research Gate.
2) Automatica, Transaction, IEEE, CSI and other journals should be educated to students and encouraged to collaborate with pursuing PhD faculty and help each other in the research domain.
3) Start research right from 2nd year and build on to final year.

➢ **Industry-Institute interaction is mostly limited to expert talks. It should be improved to have hands-on experience and working on live projects.**

PI add your suggestion to improve this point
1) Boot camps, certification course based workshops
2) Learn skills like Github and start having all your projects live online for anyone to go and see your work
3) Teach cloud based concepts for putting applications live

2) Suggestion for Center of excellence

1) Please suggest the area for Center of excellence
Big Data, Analytics, Machine Learning, DevOps using Kubernetes, Amazon Web Services, Tableau could be encouraged for making students industry ready and more company favourable

2) Please suggest the Hardware and software configuration for suggested Center of excellence
- Improve the bandwidth (network) for cloud connectivity
- Highlight practical application in industry for algorithms (eg: Hash used for credit card)
- Introduce tools (industry wide) for each subject

3) New labs suggestions

4) Please suggest the industries for Industrial visit.
get the IT parks in Pune & Bangalore. → Infosys in Mysore
in Yantra Park Thane, Quinnox (Mumbai), JP Morgan (Kalina)

5) Other Suggestions
1) Focus on techno managerial skills such as Fintech based work and collaborate with Barclays, Morgan Stanley, JP Morgan.
2) Create profiles on Codechef and other reputed coding ranking platforms to showcase in profile.

Name of DAB member : Ipsita Bhattacharya Sign : Ipsita Bhattacharya

Reach out to startups for 2nd/3rd year computer/IT projects
Target IT companies for college events sponsorships so that a better network is created to help in placements
Invite companies to publish tech articles in Fragmag to collaborate with research work
Multiple knowledge sharing sessions about new technologies

Department of Electronics and Computer Science

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

Fr. Agnel Ashram, Bandra, Mumbai 400 050

Minutes of the Meeting

Meeting: Departmental Advisory Board (DAB)

Date and Time: September 21, 2019 at 11.00am

Location: Conference Room, First floor (101)

In Attendance:

Dr. Sapna Prabhu, HOD, ECS Department, Fr. CRCE

Mr. Parag Doshi, Director, Chenao Information & Software Services Ltd.

Mr. Mustafa Fatakadawala, Tata Consultancy Services Ltd.

Mrs. Rupali Hirlekar, Larsen & Toubro Infotech Ltd.

Dr. D.V. Bhoir, PAC member, Electronics Department, Fr. CRCE

Prof. K. Narayanan, PAC member,Electronics Department, Fr. CRCE

Prof. Monica Khanore, PAC member, ECS Department, Fr. CRCE

Prof. Shilpa Patil, Programme Coordinator, ECS Department, Fr.CRCE

Agenda

1. To read out the minutes of the previous meeting
2. Discussion on the scheme of the newly introduced course, B.E. in Electronics and Computer Science
3. Suggestions on building the infrastructure in view of the reframed course
4. Discussion on the further course of action in compliance with NBA
5. Any other matter with the permission of the Chair

Head of ECS Department, Dr. Sapna Prabhu who chaired the meeting, introduced and welcomed the new members. Prof. Shilpa Patil (Program Coordinator) read out the minutes of the previous meeting.

Dr. Sapna Prabhu informed all the members that the Department has been sanctioned by AICTE the change of undergraduate course from B.E. Electronics Engineering to B.E. Electronics and Computer Science. She briefed the members about the proposed scheme of ECS syllabus.

The DAB members agreed on the following suggestions in the proposed syllabus:

1. Inclusion of
   - i) Security of code and usability in Software Engineering subject
   - ii) Mobility in Operating Systems.
   - iii) Mean stack in 4th semester laboratory course,
   - iv) Design patterns in Object Oriented programming (JAVA)
   - v) One more subject on Cloud Computing in earlier semester (In place of Analysis of Algorithm)
   - vi) Mobile databases in DBMS
   - vii) Apache Server in Computer Networks
   - viii) Virtualization in COA
   - ix) UI technologies
2. Unix operating system and Automata Theory are obsolete; hence can be removed from syllabus.
3. Conducting industry expert talks to give the students perspective of the job requirements and conducting workshops to improve students' soft skills

Mr. Parag Doshi insisted that six months internship in the industry should be included in the syllabus that will give students exposure to the real life projects and industry working environment.

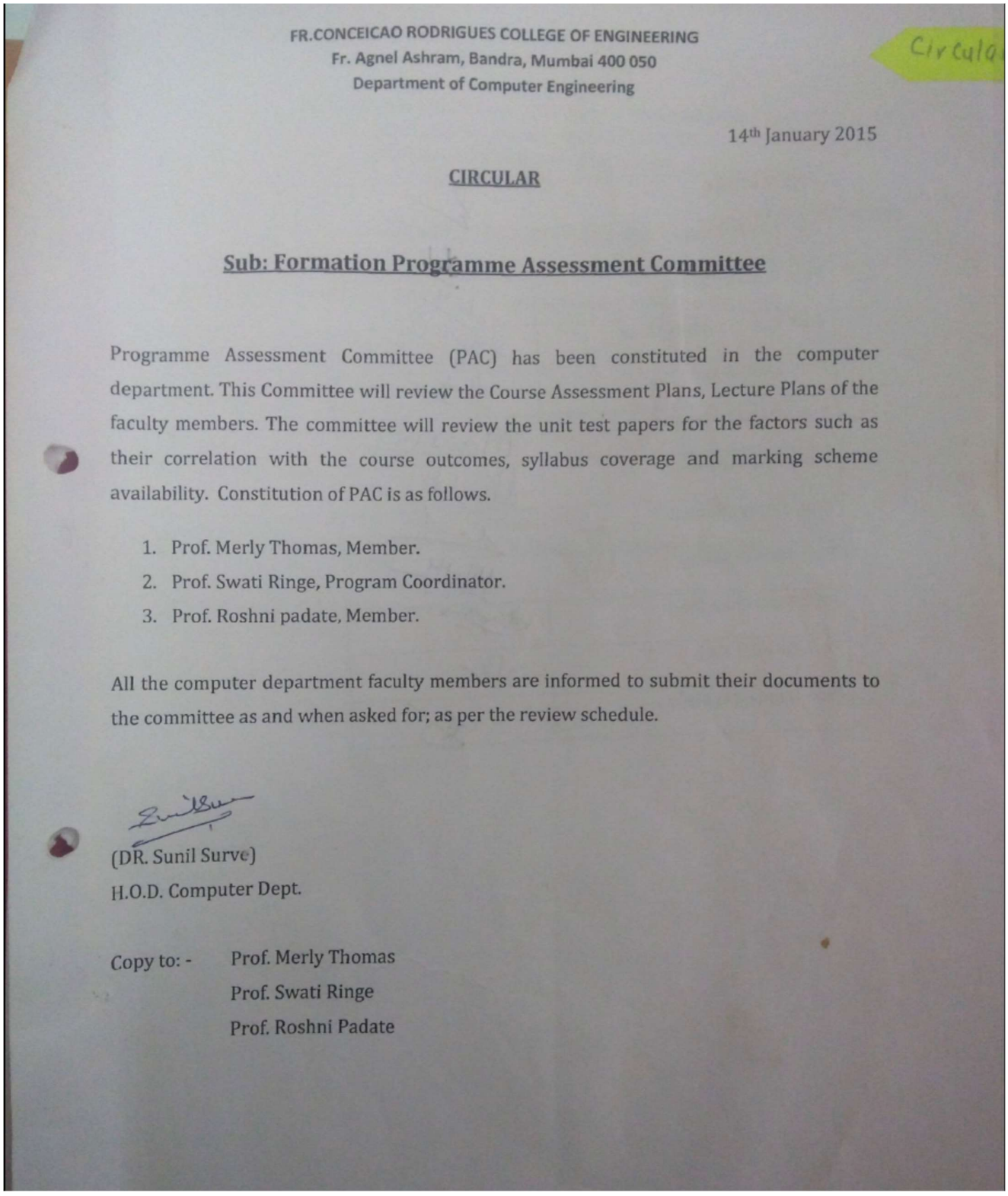
Mr. Mustafa informed about the AWS company for conducting certification courses in Cloud computing.

Regarding the infrastructure development, the DAB members expressed the need to connect the entire system to cloud, increase in bandwidth, more wifi points, availability of devices like tablets, ipad.

As Dr. Bhoir gave the overview of research projects going on in the department, Mr. Parag Doshi suggested that a team of faculty members may be formed to approve and give projects to students.

The meeting ended with vote of thanks by Dr. Sapna Prabhu.

SAMPLE – CIRCULAR PROGRAM ASSESSMENT COMMITTEE



FR.CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Fr. Agnel Ashram, Bandra, Mumbai 400 050
Department of Computer Engineering

Circular

14th January 2015

CIRCULAR

Sub: Formation Programme Assessment Committee

Programme Assessment Committee (PAC) has been constituted in the computer department. This Committee will review the Course Assessment Plans, Lecture Plans of the faculty members. The committee will review the unit test papers for the factors such as their correlation with the course outcomes, syllabus coverage and marking scheme availability. Constitution of PAC is as follows.

1. Prof. Merly Thomas, Member.
2. Prof. Swati Ringe, Program Coordinator.
3. Prof. Roshni padate, Member.

All the computer department faculty members are informed to submit their documents to the committee as and when asked for; as per the review schedule.

(DR. Sunil Surve)
H.O.D. Computer Dept.

Copy to: - Prof. Merly Thomas
Prof. Swati Ringe
Prof. Roshni Padate

RECONSTITUTION OF PAC COMMITTEE-(2019-2020)

FR.CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Fr. Agnel Ashram, Bandra, Mumbai 400 050
Department of Computer Engineering
2019-20

Date: 01/06/2019

Reconstitution of PAC committee

PAC committee is reconstituted and following are the member of PAC committee.

1) Dr. B. S. Daga, HOD Computer
2) Dr. Sunil Surve, PAC member
3) Dr. Sujata P. Deshmukh, NBA coordinator
4) Prof. Swati Ringe, PAC member
5) Dr. Sujata P. Deshmukh, PAC member
6) Prof. Merly Thomas, PAC member
7) Prof. Roshani Padate , PAC member

Following are the responsibilities of PAC members
1) Lesson plan assessment as per NBA process (Syllabus, CO, CO-PO-PSO mapping, Rubrics, list of experiments, tool, scheme)
2) Curriculum Gap and content beyond syllabus
3) Test Paper question framing as per Course CO
4) Attainment calculations

Dr. B. S. Daga
HOD Computer

SAMPLE – CIRCULAR PAC MEETING (2019-2020)

FR.CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Fr. Agnel Ashram, Bandra, Mumbai 400 050
Department of Computer Engineering

Ref/: CRCE/COMPS/2019_20/PACM/3 Date: 12/02/2020

CIRCULAR
PAC Meeting

To,
The Faculty Members,
The Department of Computer Engineering,

A PAC Meeting is scheduled to be held on 12/02/2020 at 01:30PM in the Staff Room

Date: 12/02/2020
Time: 01.30PM
Venue: Computer Lab 704 (7th floor)

Agenda:

1. CO Assessment Plan (CO Statements, Mapping, Lecture Plan, Rubrics, Tools)
2. Test1 Question papers: Correlation of question with CO
   - Subject coverage
   - Marking Scheme/Evaluation guidelines Prepared
3. Assignments Plan
4. Curriculum Gap

All the faculty members are requested to attend the meeting. Schedule is attached with this.

SIGNATURE

Dr. Sujata Deshmukh
Program Co-ordinator

SAMPLE – MINUTES OF PAC MEETING

FR.CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Fr. Agnel Ashram, Bandra, Mumbai 400 050
Department of Computer Engineering

Ref/: CRCE/COMPS/2019_20/PACMM/3

Minutes of PAC Meeting

Date: 12 Febuary 2020 **Time: 1:30PM**
Venue: Computer Lab 704 (7th floor)

Meeting was held by Program Assessment committee (PAC) with all the faculty members of Computer Engineering Department on 02nd August 2019.

Agenda:

1. CO Assessment Plan presentation(CO Statements, Mapping, Lecture Plan, Rubrics, Tools)
2. Test1 Question papers: Correlation of question with CO
   Subject coverage
   Marking Scheme/Evaluation guidelines Prepared
3. Assignments : Mapping with CO with rubrics.

Discussion and Review was done during the meeting.

1. **CO Assessment Plan submission**
   Review done on the criteria :
   CO Statements as per Blooms's Taxonomy,
   CO-PO-PSO Mappings are present,
   CO Assessment tools are present.
   Rubrics are present for all tools of assessment.
   Lecture Plan with teaching learning methods is prepared.
   The faculties are suggested some modifications at various places in the CO assessmen plan and informed to update their plans.

2. **Test1 Question papers**
   Review done on the syllabus portion for test
   Mapping of questions with CO and Evaluation guidelines are present.

3. **Assignments:**
   Review done on the Assignments for Mappings with CO and corresponding Rubrics.

SIGNATURE

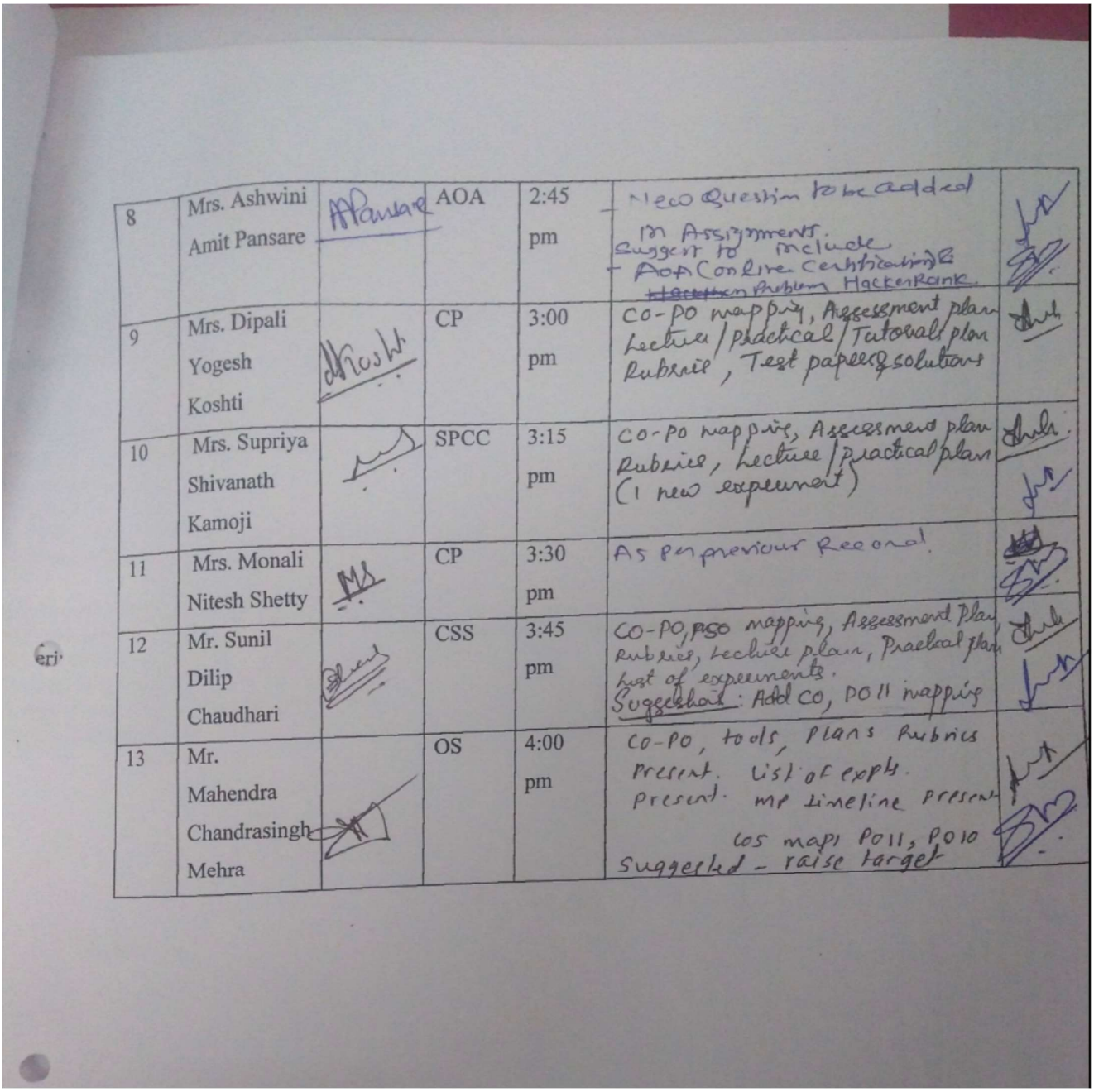
Dr. Sujata Deshmukh
Program Co-ordinator

C.C. : Dr. B. S. Daga,
Prof. Merly Thomas
Prof. Roshni Padate
Prof. Swati Ringe

Fr. Conceicao Rodrigues College of Engineering
Department of computer Engineering
2019-20
PAC Review-meeting Schedule and Report

Date: 12 /02/20202

Sr.no	Faculty Name	Sign	Subject	Time	PAC Remark	PAC sign
1	Dr. Sunil Krishnaji Surve					
2	Dr. Brijmohan Satyanarayan Daga		SE	4:30	Agile process based Model suggested in Practicals design.	
3	Dr. Sujata Deshmukh		DWM	1:30pm	use SAAS tool case study Lesson plan is evaluated with all contents	
4	Mrs. Merly Thomas Puthiyadom		DC	1:45 pm	Co. PO. PSO mapping & Lesson Plan, Practical Plan, Rubrics Assessment tool - Evaluated	
5	Ms. Roshni Suresh Padate		GG	2:00 pm	Co-po mapping, Assessment, Rubrics Lecture plans - practical plan All present	
			HMI	4:15pm	CO-PO mapping, Assessment plan Rubrics, Lecture Plan, Practical plans	
6	Mrs. Kalpana Prasanna Deorukhkar		~~CP~~ CP	2:15 pm	Co-po mapping, Lab plan, Tutorial plan, Lecture plan, Assessment Tools, Rubrics - All present	
7	Mrs. Swati Mukul Ringe		NLP	2:30 pm	CO-PO mapping, Assessment Plan Rubrics, Lecture Plan, Lab plan Practical list, Evaluation criteria Test paper — All present	
			OSTL		CO-PO mapping, Assessment, Evaluation, Lab plan, List of experiments [02 Nos] - All in course file	



8	Mrs. Ashwini Amit Pansare	APansare	AOA	2:45 pm	Neco Question to be added in Assignments. Suggest to include AOA Coursera Certification & ~~Hackerrank~~ Problem HackerRank.	
9	Mrs. Dipali Yogesh Koshti	dKoshti	CP	3:00 pm	CO-PO mapping, Assessment plan Lecture / Practical / Tutorial plan Rubrics, Test papers & solutions	
10	Mrs. Supriya Shivanath Kamoji		SPCC	3:15 pm	CO-PO mapping, Assessment plan Rubrics, Lecture / practical plan (1 new experiment)	
11	Mrs. Monali Nitesh Shetty	MS	CP	3:30 pm	As per previous Record	
12	Mr. Sunil Dilip Chaudhari		CSS	3:45 pm	CO-PO, PSO mapping, Assessment Plan Rubrics, Lecture plan, Practical plan list of experiments. Suggested: Add CO, PO 11 mapping	
13	Mr. Mahendra Chandrasingh Mehra		OS	4:00 pm	CO-PO, tools, Plans Rubrics Present. List of expts. Present. MP timeline present. COs mapi PO11, PO10 Suggested - raise target	

SAMPLE – CO ASSESSMENT PLAN

FR. Conceicao Rodrigues College Of Engineering

Father Agnel Ashram, Bandstand, Bandra-west, Mumbai-50

Department of Computer Engineering

S.E. (Computer) (semester III)

(2019-2020)

Course Outcomes & Assessment Plan

Subject: Digital Logic Design and Analysis (Course Code CSC302) **Credits-4**

Syllabus:

1. **Number Systems and Codes:**

Introduction to number system and conversions: Binary, Octal, Decimal and Hexadecimal number Systems, Binary arithmetic: addition, subtraction (1"s and 2"s complement), multiplication and division. Octal and Hexadecimal arithmetic: Addition and Subtraction (7"s and 8"s complement method for octal) and (15"s and 16"s complement method for Hexadecimal). Codes: Gray Code, BCD Code, Excess-3 code, ASCII Code. Error Detection and Correction: Hamming codes.

2. **Boolean algebra and Logic Gates**

Theorems and Properties of Boolean Algebra, Boolean functions, Boolean function reduction using Boolean laws, Canonical forms, Standard SOP and POS form. Basic Digital gates: NOT , AND , OR , NAND , NOR , EXOR , EX-NOR, positive and negative logic, K-map method 2 variable, 3 variable, 4 variable, Don"t care condition, Quine-McClusky Method, NAND-NOR Realization.

3. **Combinational Logic Design**

Introduction, Half and Full Adder, Half subtractor Full Subtractor, Four Bit Ripple adder, look ahead carry adder, 4 bit adder subtractor, one digit BCD Adder, Multiplexer, Multiplexer tree, Demultiplexer, Demultiplexer tree, Encoders Priority encoder, Decoders, One bit, Two bit , 4-bit Magnitude Comparator, ALU IC 74181.

4. **Sequential Logic Design:**

Introduction: SR latch, Concepts of Flip Flops: SR, D, J-K, T, Truth Tables and Excitation Tables of all types, Race around condition, Master Slave J-K Flip Flops, Timing Diagram, Flip-flop conversion, State machines, state diagrams, State table, concept of Moore and Mealy machine. Counters : Design of Asynchronous and Synchronous Counters,Modulus of the Counters, UP- DOWN counter, Shift Registers: SISO, SIPO, PIPO, PISO Bidirectional Shift Register, Universal Shift Register, Ring and twisted ring/Johnson Counter, sequence generator.

5. **Introduction to VHDL**

Introduction: Fundamental building blocks Library, Entity, Architecture, Modeling Styles, Concurrent and sequential statements, simple design examples for combinational circuits and sequential circuits

6. **Digital Logic Families**

Introduction: Terminologies like Propagation Delay, Power Consumption, Fan in and Fan out , current and voltage parameters, noise margin, with respect to TTL and CMOS Logic and their comparison

Course Objectives (optional):

1. To introduce the fundamental concepts and methods for design of digital circuits and a pre-requisite for computer organization and architecture, microprocessor systems.
2. To provide the concept of designing Combinational and sequential circuits.
3. To provide basic knowledge of how digital building blocks are described in VHDL.

Course Outcomes:

Upon completion of this course students will be able to:

CSC302.1: Perform number system and code conversions. (**Comprehension**)
CSC302.2: Design combinational circuits. (**Apply**)
CSC302.3: Design sequential circuits. (**Apply**)
CSC302.4: Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design. **(Analyze , Apply)**

Mapping of CO and PO/PSO

Relationship of course outcomes with program outcomes: Indicate 1 (low importance), 2 (Moderate Importance) or 3 (High Importance) in respective mapping cell.

	PO1 (Engg Know)	PO2 (Ana)	PO3 (De sign)	PO4 (inve stiga)	PO5 (tools)	PO6 (engg Soci)	PO7 (Env)	PO8 (Eth)	PO9 (ind Team)	PO10 (com.)	PO11 (PM)	PO12 (life Long)
CSC302.1	3											
CSC302.2	3	2	3		1							
CSC302.3	3	2	3		1							
CSC302.4	3	3	3		3				2	2		
Course To PO	3	2.6	3		1.6				2	2		

CO	PSO1	PSO2
CSC302.1	3	
CSC302.2	3	
CSC302.3	3	
CSC302.4	3	
Course to PSO	3	

Justification

PO1: All COs are mapped to PO1 because engineering graduates will be able to apply the knowledge of **mathematics** & **Digital electronics fundamentals** to solve complex engineering problems.

Level 3 - The course demands mathematical concept to be applied to solve given problems. Also basic knowledge of digital electronics and fundamental of computer system is required.

PO2: CSC302.2, CSC302.3 and CSC302.4 are mapped to PO2 because the students **analyze** the given problem statement before designing the actual circuit.

Level 2 – CSC302.2 & CSC302.3 **Before designing any circuit for the given problem, students perform basic level of pre-analysis. (Analysis Includes identifying inputs - outputs, deriving truth table, minimization of output expression, Identify method for minimization, identify components to be used)**

Level 3 – CSC302.4 **– In order to provide a solution to a real world chosen problem, students design and then analyze the behavior of a circuit. Here students do rigorous analysis to obtain the desired output.**

PO3: CSC302.2, CSC302.3 and CSC302.4 are mapped to PO3 because the students **design** the digital circuits and implement them using hardware components.

Level 3: Because the course involves designing of various combinational and sequential circuits, students actually design the circuit and implement it in laboratory.

PO5:

CSC302.2 and CSC302.3 are mapped to PO5 because students use advance tool such as VHDL to analyze the basic combinational and sequential circuit.

Level 1 -Since basic analysis is done using VHDL.

CSC302.4 maps to PO5 because the students use various tools for example VHDL, Arduino Uno various actuators and sensors etc. to simulate/implement a real world problem.

Level 3 - Since students translate real world problem to digital network and analyze the circuit using various tools ; the nature of the problem is more complex here.

PO9: CSC302.4 is mapped to PO9 because the students work in a **team** to design and implement a solution for a chosen real world problem.
Level 2 - Since it's a mini project that give them first level of experience of being in a team; not rigorous team work is involved. Hence level is 2.

PO10: CSC302.4 is mapped to PO10 because the students explain mini project by demonstrating the project and also submit written report for the same.
Level 2 – basic level of presentation skills and written skills are expected.

PSO1: All COs are mapped to PSO1 because the graduates will be able to apply knowledge of Digital Electronics to simulate the real world problem.

Course Outcomes Target:

Upon completion of this course students will be able to:

CSC302.1: Perform number system and code conversions. (**Comprehension**)
CSC302.2: Design combinational circuits. (**Apply**)
CSC302.3: Design sequential circuits. (**Apply**)
CSC302.4: Simulate real world problems using VHDL. **(Analyze & Apply)**

Target:

CSC302.1: 2.5
CSC302.2: 2.5
CSC302.3: 2.5
CSC302.4: 2.5

Previous Years' Achievements

CO	Year 2018-19	Year 2017-18
CSC302.1	1.88	2.36
CSC302.2	2.2	2.2
CSC302.3	2.36	2.04
CSC302.4	3	2.44

CO Assessment Tools:

CSC302.1: Perform number system and code conversions

Direct Methods(80%): Test 1 + Module Test 1 + Quiz1 + UniExamTh + UniExam Pr

CO1dm = 0.2T1 + 0.2 MT+ 0.2 Q1 + 0.2UTh + 0.2 UPr

InDirect Methods(20%): Course exit survey

CO1idm

CSC302.1 = 0.8*CO1dm + 0.2* CO1idm

Direct Methods	Weightage	Target	Date	Marks
Test 1	0.2	**65%** students will score minimum 65% marks (i.6. 6 or more out of 10)		Q-1 (08M)
Module Test1	0.2	70% students will score minimum 70% marks (i.e. 7 or more out of 10)	4th week of July	10M
Quiz1	0.2	**65%** students will score minimum 70% marks (i.6. 14 or more out of 20)	4th week of July	20M
Uni Theory exam	0.2	60% students will score minimum 60% marks (i.6. 48 or more out of 80)		80M
Uni. Practical Exam	0.2	60% students will score minimum 70% marks (i.6. 17.5 or more out of 25)		25M

CSC302.2: Design combinational circuits.

Direct Methods(80%): (Test1+Test2) + Lab + Assignment1 + UniExamTh + UniExam Pr

CO2dm = 0.2T1 + 0.2Lab + 0.2A1 + 0.2UTh +0.2UPr

InDirect Methods(20%): Course exit survey

CO2idm

CSC302.2 = 0.8*CO2dm + 0.2* CO2idm

Direct Methods	Weightage	Target	Date	Marks
Test	0.2	60% students will score minimum 60% marks (i.6. score 9 or more out of 15)	T1-14/8/19	**18M** Q-2(8)+Q-3(4) in T1 & Q-1 (6M) T2
Lab	0.2	70% students will score minimum 70% marks.(i.e score 56 or more out of 80)	Exp 1 to 7 & Exp 11	80M
Assignment1	0.2	**70%** students will score minimum 70% marks (i.6. score 07 or more out of 10)		10M
Uni Theory exam	0.2	60% students will score minimum 60% marks (i.6. 48 or more out of 80)		80M
Uni. Practical Exam	0.2	60% students will score minimum 70% marks (i.6. 17.5 or more out of 25)		25M

CSC302.3: **Design sequential circuits.**

Direct Methods(80%): Test2 + Module Test 2 + Lab + UniExamTh + UniExamPr

CO3dm = 0.2T2 + 0.2M2 +0.2Lab + 0.2UTh + 0.2UPr

InDirect Methods(20%): Course exit survey

CO3idm

CSC302.3 = 0.8*CO3dm + 0.2* CO3idm

Direct Methods	Weightage	Target	Date	Marks
Test 2	0.2	60% students will score minimum 60% marks (i.6. score 9 or more out of 15)	T2- 15/10/19	14M [Q2(6) + Q3(8)] in T2
Lab	0.2	70% students will score minimum 70% marks.(i.e score 28 or more out of 40)	EXP 8,9,10 & 12	40M
Module Test 2	0.2	60% students will score minimum score 60% marks (i.e. score 12 or more out of 20)	1st week of October	20M
Uni Theory exam	0.2	60% students will score minimum 60% marks (i.6. 48 or more out of 80)		80M
Uni. Practical Exam	0.2	60% students will score minimum 70% marks (i.6. 17.5 or more out of 25)		25M

CSC302.4: Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design.

Direct Methods(80%): MiniProject , lab

CO4dm = 0.2 Lab + 0.8 MP

InDirect Methods(20%): Course exit survey

CO4idm

CSC302.4 = 0.8*CO4dm + 0.2* CO4idm

Direct Methods	Weightage	Target	Date	Marks
Lab	0.2	70% students will score minimum 70% marks.(i.e score 14 or more out of 20)	Exp. 3-12	100M
Mini Project	0.8	60% students will score minimum 70% marks.(i.e score 10.5 or more out of 15)	Submission: 1st and 2nd week of October	15M

Content Beyond Syllabus:

Introduction to IoT

Curriculum Gap:

Indicator	Poor	Average	Good	Excellent

- Introduction to 8085 Processor to get better and practical applications of registers and ALU.
- In order to understand current applications, trends and new directions in logic design following topics shall be covered.

Sr.No.	Curriculum gap contents	Action Plan
1	Introduction to IOT	Self-learning online resource is provided on Moodle and flip class room activity.

List of Experiments with CO mapping

Sr. No	Title	CO
1.	To study and verify the truth table of various logic gates using ICs and realize Boolean expressions using gates.	CSC302.2
2.	To realize basic gates using universal gates.	CSC302.2
3.	To realize arithmetic circuits i) Half adder ii) Full adder iii) Half subtractor iv) Full subtractor.	CSC302.2
4.	To realize binary to gray code and gray code to binary converter.	CSC302.2
5	To realize parity generator and detector.	CSC302.2
6.	To Study multiplexer IC and realization of full adder using multiplexer IC	CSC302.2
7.	To realize 2 bit magnitude comparator.	CSC302.2
8.	Study of flip-flops using IC's	CSC302.3
9.	To realize shift registers using flip flops	CSC302.3
10.	To realize asynchronous 3 bit up counter.	CSC302.3
11	To realize combinational circuit using VHDL	CSC302.2
12.	To realize basic Sequential circuit using VHDL	CSC302.3
13.	Mini Project – Design and Implement a real world problem using learned concepts of digital Electronics	CSC302.4

Rubrics for Experiments:

Timeline (2)	More than two session late (0)	Two sessions late (1)	One session late (1.5)	Early or on time (2)
Analysis of problem and Circuit optimization (2)	Failed to do proper analysis , Very complex circuit(0.5)	Analysis done. The circuit is structured but unnecessary lengthy (1.5)	N.A.	Detailed analysis done. The circuit is structured and efficient.(2)
Output (4)	Failed to implement a complete design. Partial implementation. No output (1)	Hardware implementation done but failed to show output due to some error. (2)	Hardware implementation done. Output shown but some of the test cases not working. (3)	Expected output shown. All test cases verified. (4)
PostLab Assignment (2)	Not able to solve(0)	Able to solve 25% (1)	Able to solve 50%(1.5)	Able to solve all questions(2)

Rubrics for the Mini Project:

Mini project that covers design and implementation of important Digital circuits' concepts of the course, is allotted to the students in groups. The requirements will be announced in advance and discussed in class. The students' progress on their project will be discussed in the practical session and faculty office. Finally at the time of submission the students will present the demonstration of their project in lab session and submit a report for the same.

Indicator	Poor	Average	Good	Excellent
Timeline Maintains project deadline (2)	More than two session late (0.5)	Two sessions late (1)	One session late (1.5)	Early or on time (2)
Completeness Complete all parts of project (3)	< 40% complete (1)	~ 60% complete (2)	~ 80% complete (2.5)	100% complete(3)
System Design (3) Block diagram And circuit realization	NA	Designed circuit with basic gates (2)	Designed with NAND or NOR but not minimum (2.5)	Correct Designed with NAND or NOR Logic (3)
Report Submission(2)	N/A	Submitted one session late (1)	Partial steps are followed (1.5)	All steps are followed and well documented (2)

Schedule of mini project submission:

Stages of mini project	Date of submission
Project topic submission	16-Sep-2019
Analysis submission	23-Sep-2019
Design Submission	30-Oct-2019
Implementation	Second week of October

Rubrics for Assignments:

Indicator	Very Poor	Poor	Average	Good	Excellent
Timeline (2)	Assignment not submitted (0)	More than one week late (0.5)	Two weeks late (1)	One week late (1.5)	Early or on time (2)
Organization (2)	N/A	Very poor readability and not structured (0.5)	Poor readability and somewhat structured (1)	Readable with one or two mistakes and structured (1.5)	Very well written and structured without any mistakes (2)
Solution (3)	N/A	All solutions incorrect (0)	More than 50% Solutions are incorrect (1)	20-30% solutions incorrect (2)	All problems solved correctly (3)
Depth and breadth discussion (3)	N/A	None in evidence; superficial at most (0.5)	Minor points/information may be missing and discussion is minimal (1)	Discussion centers on some of the points and covers them adequately (2)	Information is presented in depth and is accurate (3)

Assignments:

ASSIGNMENT 1:

Date of Assignment: 30-08-2019
Date of submission: 12-09-2019 Year: 2019-2020
Maps to CSC302.2: Design Combinational circuits

Real world problems:

Q-1 A step in space vehicle checkout depends on 4 sensors s1, s2, s3 and s4. Circuit is properly working if sensors s2 and at least two of the other three sensors are at logic 1. Implement the system.

Q-2 Design a circuit with 4 inputs that has outputs with a binary value equal to the number of inputs that are HIGH.

Q-3 Design a combinational logic circuit with a single output that will serve as an "auto buzzer circuit in a car. The circuit should output a HIGH signal (to sound a buzzer) for each of the following conditions:

1) A driver's DOOR is open and the KEYS are in the ignition.
2) If the SEAT is occupied and the SEATBELTS are not buckled and the KEYS are in the ignition.

Determine the truth table for the circuit described above. Determine the minimal circuit and draw it using NAND gates only.

[Hint: A – Door (1 - open , 0 - closed) , B – KEYS (1 – in ignition , 0 – Not in ignition), C – SEAT (1- occupied, 0 not occupied), D – SEAT BELT (1 – buckled, 0 – not buckled)]

Q-4 A bank wants to design an alarm system for its safety. The alarm will sound.....

1) If bank is open (B=1) and there is a robbery (R=1) , alarm at bank (BA=1) and police station (PA=1) will sound.
2) If bank is closed (B=0) and there is a robbery (R=1), alarm will sound at police station only (PA=1).
3) If there is a fire (F=1) while the bank is open (B=1) , the alarm will sound in the in the bank (BA=1) and fire station (FA=1).
4) If there is fire (F=1) while the bank is closed (B=0), alarm will sound at fire station (FA=1) only.

Determine the truth table and design the circuit using basic gates (AND, OR, NOT, EXOR etc).

Design problems:

Q-5 Design 4- bit BCD subtractor using 4-bit parallel adder (IC 7483).

Q-6 Design BCD to seven segment display decoder.

Q-7 Design a combinational logic circuit that will multiply two 2-bit numbers.

Q-8 Simplify using Quine's McCluskey method. $F(A,B,C,D) = \Sigma m(0,1,4,5,9,10,12,14,15) + \Sigma d(2,8,13)$.

Verify your answer using KAMP.

Q-9 Design **32:1 MUX** using **4:1 MUX**. How many MUX do you need?

Q-10 Design 24-bit magnitude comparator using IC 7485.

Q-11 Implement following Boolean function using 4:1 MUX. F(A,B,C,D,E) = Σm(0,1,2,3,6,8,9,10,13,15,17,20,24)

Module Test 1:

Class: S.E. Comp (Sem III) **Date: 26-07-2019**

Subject : DLDA **Time : 11:00 to 12:00**

Maps to CO1: Perform number system conversion

Set-1

Q-1 Convert decimal number 576.24 into Binary, ,octal, base 9 and Hexadecimal. [04]

Q-2 Construct Hamming code for 1010 using odd parity. [04]

Q-3 Convert (-89) into equivalent signed magnitude, 1'complement and 2'scomplement form [04]

Q-4 Perform subtraction using 2's complement. $(62)_{10} - (99)_{10}$ [04]

Q-5 Perform subtraction using 16's complement [04]

i) $(CB1)_{16} - (971)16$
ii) $(426)_{16} - DBA)_{16}$

Set -2

Q-1 Convert decimal number 1762.46 into Binary, octal , base 7 and Hexadecimal. [04]

Q-2 Construct Hamming code for 1010 using even parity. [04]

Q-3 Convert (-80) into equivalent signed magnitude, 1'complement and 2'scomplement form [04]

Q-4 Convert $(47.3)_{10}$ to Gray code [04]

Q-5 Perform Following [04]

i) addition of $(34)_8$ and $(62)_8$.
ii) Perform $(289)_H - (1AD)_H$ without converting to any other base.

Module Test 2:

Brach/ Semester: Computer/III — Date: 09-10-2019

Course: DLDA (CSC302) — Duration: 1 Hr.

Q-1 Implement following logic function using 8:1 Mux. [06]

$F(A,B,C,D) = \Sigma m(1,3,5,10,11,13,14)$

Q-2 Design Mod – 6 asynchronous counter. Also draw timing diagram. [07]

Q-3 Design MOD-6 synchronous counter using T flipflops. [07]

OR

Q-3 Design synchronous counter for the following sequence

0-> 1 -> 3 -> 4 -> 6 -> 0

FR. Conceicao Rodrigues College Of Engineering

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Department of Computer Engineering

S.E. (Computer) (semester III)

Lesson Plan : Digital Logic Design And Analysis

Semester III **Year: 2019-20**

Modes of Content Delivery:

i	Class Room Teaching	v	Self Learning Online Resources	Ix	Industry Visit
ii	Tutorial	vi	Slides	X	Group Discussion
iii	Remedial Coaching	vii	Simulations/Demonstrations	xi	Seminar
iv	Lab Experiment	viii	Expert Lecture	xii	Case Study

Lect. No.	Portion to be covered	Planned date	Actual date	Content Delivery Method/Learning Activities	Reference material
	MODULE 1: Number Systems and Codes				
1.	Introduction to the subject, Revision of Binary, Octal, Decimal and Hexadecimal number Systems.	1/7/19	1/7/19	Class Room Teaching	i
2	Number system conversion and Numerical on number system conversion	3/7/19	3/7/19	Class Room Teaching	i
3	Number system conversion and Numerical on number system conversion	4/7/19	4/7/19	Class Room Teaching	i
4	Binary Arithmetic: Binary Addition and Subtraction (1's complement and 2's complement)	5/7/19	5/7/19	Class Room Teaching	i
5	Multiplication & Division	8/7/19	8/7/19	Class Room Teaching	I
6	Octal and Hexadecimal arithmetic	10/7/19	10/7/19	Class Room Teaching	I
7	Codes: Gray, BCD, Excess 3 , ASCII Code	11/7/19	11/7/19	Class Room Teaching	I

8	Error Detection and correction codes: Hamming codes :	**12/7/19**	**12/7/19**	Class Room Teaching	i, iv
	MODULE 2:Boolean Algebra and Logic Gates				
9	Theorem and properties of Boolean algebra. Boolean functions and function reduction using Boolean laws.	**16/7/19**	**16/7/19**	Class Room Teaching	i
10	Canonical forms: SOP ,POS	**17/7/19**	**17/7/19**	Class Room Teaching	I,iv
11	Basic Digital gates: NOT , AND , OR , NAND , NOR , EXOR , EX-NOR, positive and negative logic. NAND-NOR Realization	**18/7/19** (cancelled due to talk)	**19/7/19**	Class Room Teaching **[Video1]** **[TPS activity]**	i, iv
12	K-map method 2 variable, 3 variable, 4 variable, Don‟t care condition	**19/7/19**	**22/7/19**	Class Room Teaching	i, iv
13	K-map method 2 variable, 3 variable, 4 variable, Don‟t care condition.	**23/7/19**	**23/7/19**	Class Room Teaching	i, iv
14	Solving more problems using K-Maps and	**24/7/19**	**24/7/19**	Class Room Teaching **[TPS activity]**	i, iv
15	Quine-McClusky Method, NAND-NOR Realization.	**25/7/19**	**25/7/19**	Class Room Teaching	i, iv
16	Quine-McClusky Method Quine-McClusky Method. NAND-NOR Realization.	**26/7/19**	**25/7/19**	Class Room Teaching	i, iv
17	**Module Test1 -1**	**30/7/19**	**26/7/19**		
	Module 3: Combinational Logic Design				
18	Introduction to combinational logic, Half Adder , Full Adder	**31/7/19**	**30/7/19**	Class Room Teaching	i
19	Half Subtractor , Full subtractor	**1/8/19**	**31/7/19**	Class Room Teaching	i
20	Four Bit Ripple adder, look ahead carry adder, 4 bit adder subtractor	**2/8/19**	**2/8/19**	Class Room Teaching	I
21	Code converters : Binary to Gray, Gray to Binary, BCD to Binary, Binary to BCD	**6/8/19**	**6/8/19**	Class Room Teaching, Lab	i, iv

				Experiment	
22	Code converters: BCD to EX-3, EX-3 to BCD	**7/8/19**	**7/8/19**	Class Room Teaching	i, iv
23	One digit BCD Adder, One digit BCD Subtractor	**8/8/19**	**8/8/19**	Class Room Teaching	i
24	Encoders, Priority encoder, Decoders	**9/8/19**	**9/8/19**	Class Room Teaching	i, iv
25	Multiplexer, Multiplexer tree	**20/8/19**	**20/8/19**	Class Room Teaching, Lab Experiment	i, iv
26	Demultiplexer, Demultiplexer tree	**21/8/19**	**21/8/19**	Class Room Teaching	i, iv
27	One bit, Two bit, 4-bit Magnitude Comparator, ALU IC 74181.	**22/8/19**	**22/8/19**	Class Room Teaching, Lab Experiment	i, iv
	Module 4: Sequential Logic Design				
28	Introduction: SR latch , Concepts of Flip Flops: SR, D, J-K, T,	**23/8/19**	**23/8/19**	Class Room Teaching **[video2]**	I
29	Truth Tables and Excitation Tables of all types, Race around condition	**27/8/19**	**27/8/19**	Class Room Teaching, Lab Experiment	I
30	Master Slave J-K Flip Flops, Timing Diagram,	**28/8/19**	**28/8/19**	Class Room Teaching	I
31	Flip-flop conversion	**29/8/19**	**29/8/19**	Class Room Teaching	i, iv
32	Shift Registers: SISO, SIPO, PIPO, PISO	**30/8/19**	**1/9/19**	Class Room Teaching	i, iv
33	Bidirectional Shift Register	**11/9/19**	**13/9/19**	Class Room Teaching	i, iv
34	Universal Shift Register	**12/9/19**	**17/9/19**	Class Room Teaching, Lab	i, iv

				Experiment	
35	Ring and twisted ring/Johnson Counter	**13/9/19**	**18/9/19**	Class Room Teaching	i, iv
36	State machines, state diagrams, state tables. Concept of Moore and Mealy machine.	**17/9/19**	**18/9/19**	Class Room Teaching	i, iv
37	Counters: Design of Asynchronous Counters	**18/9/19**	**19/9/19**	Class Room Teaching, Lab Experiment **[Video3]**	i, iv
38	Counters: Design of Synchronous Counters	**19/9/19**	**20/9/19**	Class Room Teaching	i,iv
39	Modulus of the Counters	**20/9/19**	**24/9/19**	Class Room Teaching	i,iv
40	UP- DOWN counter	**24/9/19**	**25/9/19**	Class Room Teaching	i,iv
41	Sequence generator.	**25/9/19**	**26/9/19**	Class Room Teaching	i,iv
	Module 5: Introduction to VHDL				
42	Introduction: Fundamental building blocks Library, Entity	**26/9/19**	**3/10/19**	Class Room Teaching, **slides**	iii,v
43	Architecture, Modeling Styles	**27/9/19**	**3/10/19**	Class Room Teaching, **slides**	iii,v
44	Concurrent and sequential statements.	**30/9/19**	**4/10/19**	Class Room Teaching, **slides**	iii,v
45	simple design examples for combinational circuits, simple design examples for Sequential circuits.	**1/10/19**	**4/10/19**	Class Room Teaching, Lab Experiment	iii,v
	Module 6: Digital Logic Families				
46	Introduction: Terminologies like Propagation Delay, Power Consumption, Fan in and Fan	**3/10/19**	**9/10/19**	Class Room Teaching	I

	out , current and voltage parameters, noise margin,				
47	Comparison of TTL and CMOS Logic	**4/10/19**	**9/10/19**	Class Room Teaching	I
48	Flipped class room activity for ½ an hour and University Question papers Solution for ½ an hour	**5/10/19**	**11/10/19**	Class Room Teaching	

Resource	Topic	Source	Type
Video1	Transistors and Boolean logic	https://www.youtube.com/watch?v=SW2Bwc17_wA	You tube
Video2 Animation	RS Flip Flop	https://www.youtube.com/watch?v=--pv3MZMoo0	You tube
Video3	Introduction to counter	https://www.youtube.com/watch?v=iaIu5SYmWVM	You tube

Text Books/ Reference Books:

Te x t B o o k s :

Text Books:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.

2. Yarbrough John M. , "Digital Logic Applications and Design ", Cengage Learning

3. J. Bhasker." VHDL Primer", Pearson Education

Reference Books:

4. M. Morris Mano, "Digital Logic and computer Design", PHI.

5. Douglas L. Perry, "VHDL Programming by Example", Tata McGraw Hill.

6. Donald p Leach, Albert Paul Malvino,"Digital principles and Applications", Tata McGraw Hill.

FR. Conceicao Rodrigues College Of Engineering

Father Agnel Ashram, Bandstand, Bandra-west, Mumbai-50

Department of Computer Engineering

S.E. (Computer) (semester III)

(2019-2020)

LABORATOTY PLAN: DIGITAL SYSTEM LAB

Semester III **Year: 2019-20**

Sr. No	Title	CO	Planned dates	Actual dates			
	BATCH →			A	B	C	D
1.	To study and verify the truth table of various logic gates using ICs and realize Boolean expressions using gates.	CSC302.2	3rd week of July	17/7/19	16/7/19	15/7/19	15/7/19
2.	To realize basic gates using universal gates.	CSC302.2	4th week of July	24/7/19	23/7/19	22/7/19	22/7/19
3.	To realize arithmetic circuits i) Half adder ii) Full adder iii) Half subtractor iv) Full subtractor.	CSC302.2	1st week of August	31/7/19	30/7/19	29/7/19	29/7/19
4.	To realize binary to gray code and gray code to binary converter.	CSC302.2	2nd week of August	7/8/19	6/8/19	6/8/19	6/8/19
5	To realize parity generator and detector. (New)	CSC302.2	4th week of August	21/8/19	20/8/19	20/8/19	20/8/19
6.	To Study multiplexer IC and realization of full adder using multiplexer IC.	CSC302.2	1st week of September	28/8/19	27/8/19	27/8/19	27/8/19
7.	To realize 2 bit magnitude comparator.	CSC302.2	1st week of September	28/8/19	27/8/19	27/8/19	27/8/19
8.	Study of flip-flops using IC's	CSC302.3	2nd week of September	11/9/19	17/9/19	16/9/19	16/9/19
9.	To realize shift registers using flip flops	CSC302.3	2nd week of September	18/9/19	17/9/19	24/9/19	24/9/19
10.	To realize asynchronous 3 bit up counter.	CSC302.3	3rd week of September	25/9/19	24/10/19	30/9/19	30/9/19
11	To realize combinational circuit using VHDL	CSC302.2 CSC302.4	3rd week of September	9/10/19	1/10/19	7/10/19	7/10/19
12.	To realize basic Sequential circuit using VHDL	CSC302.3 CSC302.4	4th week of September	9/10/19	1/10/19	7/10/19	7/10/19
13.	Mini Project	CSC302.4		Submission 2nd week of October			

SAMPLE – GUEST LECTURE (2019-2020)

Web Design Lab

Expert lecture on **BOOTSTRAP**
Subject In charge: Prof. Mahendra Mehra
Class: TE Computers
Semester: V

Agenda?

- Creating an effective web-based Resume for Placements.
- Hosting the web-based resume on GitHub pages.
- Benefits of GitHub Student Developer pack.

PREREQUISITE: Basics of HTML, CSS and JAVASCRIPT
Date: Sunday, 2nd August 2020.
Time: 3:00 Pm to 4:00 Pm
Meeting ID: https://meet.google.com/zjp-mgrg-ynj

Scan Me to Join

"Creative solutions, creative results."

Mr. Rathil Patel
Solution Engineer,
Browserstack

www.frcrce.ac.in

SAMPLE – CO ATTAINMENT

(2019-2020)

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**
CSC302.1 : **Perform number system and code conversions** **Target : 2.5**

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
TEST	0.2	No. of students scoring >= 4.8 out of 8 in Q-1 (T1)	60	84.51	3	0.6
60% students will score minimum 60% marks						
MODULE TEST1	0.2	No. of students scoring >=14 out of 20 in ass1	47	71.21	1	0.2
70% students will score minimum 70% marks						
QUIZ	0.2	No. of students scoring >=14 out of 20 in Quiz1	58	81.69	2	0.4
65% students will score minimum 70% marks						
UNI THEORY	0.2	No. of students acoring >= 48 out of 80	50	70.42	2	0.40
60% students will score minimum 60% marks						
UNI PRACTICAL	0.2	No. of students acoring >= 17.5 out of 25	70	98.59	3	0.6
60% students will score minimum 70% marks						
INDIRECT METHOD						**2.2**
Course Exit Survey	1	No. of students agree + strongly agree	65	1	3	3
75% students will score minimum 75% marks		No. of respondents = 65				
No. of students	**71**					

Levels	Test	QUIZ	Module Test	End sem exam(TH)	End sem exam(PR)	Survey
1 (Low)	60-69	65-74	70-79	60-69	60-69	75-80
2 (Medium)	70-79	75-84	80-89	70-79	70-79	81-85
3 (High)	80 and above	85 and above	90 and above	80 and above	80 and above	86 above

CO1 Attainment = 2.36

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**

CSC302.2: Design combinational circuits **Target : 2.5**

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
TEST (T1+T2)	0.2	No. of students scoring >= 10.8 out of 18 in Q-2(8)+Q-3(4) in T1 & Q-1 (6M) T2	47	66.20	1	0.2
60% students will score minimum 60% marks						
LAB	0.2	No. of students scoring >=56 out of 80 in exp1-7,11	70	98.59	3	0.6
70% students will score minimum 70% marks						
ASSIGNMENT	0.2	No. of students scoring >=14 out of 20 in Quiz1	69	97.18	3	0.6
60% students will score minimum 70% marks						
UNI THEORY	0.2	No. of students acoring >= 48 out of 80	50	70.42	2	0.4
60% students will score minimum 60% marks						
UNI PRACTICAL	0.2	No. of students acoring >= 17.5 out of 25	70	98.59	3	0.6
60% students will score minimum 70% marks						
INDIRECT METHOD						**2.4**
Course Exit Survey	1	No. of students agree + strongly agree	65	1	3	3
75% students will score minimum 75% marks		No. of respondents = 65				
No. of students	**71**					

Levels	Test	ASSIGNMENT	LAB	End sem exam(TH)	End sem exam(PR)	Survey
1 (Low)	60-69	60-69	70-79	60-69	60-69	75-80
2 (Medium)	70-79	70-79	80-89	70-79	70-79	81-85
3 (High)	80 and above	80 and above	90 & above	80 and above	80 and above	86 above

CO2 Attainment = 2.52

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**
CSC302.3 : Design sequential circuits. **Target : 2.5**

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
TEST (T2)	0.2	No. of students scoring >= 9 out of 14 in Q2(6) + Q3(8) in T2	31	43.66	0	0
60% students will score minimum 60% marks						
LAB	0.2	No. of students scoring >=28 out of 40 in exp8,9,10,12	70	98.59	3	0.6
70% students will score minimum 70% marks						
MODULE TEST2	0.2	No. of students scoring >=14 out of 20 in Quiz1	57	80.28	3	0.6
60% students will score minimum 70% marks						
UNI THEORY	0.2	No. of students acoring >= 48 out of 80	50	70.42	2	0.4
60% students will score minimum 60% marks						
UNI PRACTICAL	0.2	No. of students acoring >= 17.5 out of 25	70	98.59	3	0.6
60% students will score minimum 70% marks						
INDIRECT METHOD						2.2
Course Exit Survey	1	No. of students agree + strongly agree	65	1	3	3
75% students will score minimum 75% marks		No. of respondents = 65				
No. of students	**71**					

Levels	Test	Module Test	LAB	End sem exam(TH)	End sem exam(PR)	Survey
1 (Low)	60-69	60-69	70-79	60-69	60-69	75-80
2 (Medium)	70-79	70-79	80-89	70-79	70-79	81-85
3 (High)	80 and above	80 and above	90 & above	80 and above	80 and above	86 above

CO3 Attainment = 2.36

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**

CSC302.4: Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design
Target : 2.5

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
LAB	0.2	No. Of students scoring 14 or more out of 20 in EXP 11,12	71	1.00	3	0.6
70% students will score minimum 70% marks						
MINI PROJECT	0.8					
65% students will score minimum **70%** marks		No. of students score 10.5 or more out of 15 =	71	1.00	3	2.4
						3
INDIRECT METHOD						
Course Exit Survey	1	No. of students agree + strongly agree	64	0.98	3	3
		No. of respondents = 65				

Level	Lab	Mini Project
1	70-79	65-74
2	80-89	75-84
3	90 & above	85 and above

CSC302.4 Attainment = 3

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)

BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**

CO	Description	Attainment
CSC302.1	Perform number system and code conversions	2.36
CSC302.2	Design combinational circuits	2.52
CSC302.3	Design Sequential circuits	2.36
CSC302.4	Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design	3

PO Attainment

CO Number	Course Outcome	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	CO Attain
CSC302.1	Perform number system and code conversions	3												3		2.36
CSC302.2	Design combinational circuits.	3	2	3	1									2		2.52
CSC302.3	Design sequential circuits.	3	2	3	1									3		2.36
CSC302.4	Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design	3	3	3	3					2	2			3		3
Total		12	7	9	5					2	2			11		
CO-PO MATRIX		3	2.33	3.00	1.67					2	2			2.75		
PO ATTAINMENT		1.92	2.77	2.6	2.86					3	3			2.55		

BE – FINAL YEAR PROJECT ASSESSMENT

BE - PROJECTS - PLAN

Fr. Conceicao Rodrigues College of Engineering

Department of Computer Engineering

2019-2020

Project Activity Schedule

B.E Computer Engineering

Date/week	Activity	Class
First week of May/End of April	Project Idea Submission Notice for Students and faculty Period for idea submission- Till 3July 2019	TE -6
BE-7 Activities		
July 1/2 week (08/072019)	Project topic approval Presentation	BE-7
July 3 / 4 week (24/07/2019)	Assigning guides to Project	
August1/2 week (Till 03/08/2019)	Final project problem definition with guide(with research Papers)- Assigning new topics to Rejected project topic based on project idea submitted by faculties/ revision of Problem definition	
September 2/3 week (11/09/2019)	**Mid term Presentation1** with research Papers and work attempted 40%	BE-7
October 1/2 week (05/10/2019)	**Mid term Presentation2** with work attempted 80%	BE-7
October 2/3week	Report submission and 100% work done	BE-7
As per university schedule	Oral exam and TW report evaluation	BE-7
BE-8 Activities		
February 1 / 2 week (10/02/2020)	**Mid term Presentation1**- 1)Rough draft1 of research paper 2)Product features specifications with market research 3) Abstract submission to conferences or Journals	BE-8
March 1 / 2 week	**Mid term Presentation2** - 1)Final draft2 of research paper 2)Product features Implementation 3) Final paper submission to conferences or Journals	BE-8
March 3 / 4week	1)Implementation /demo to guide- Possibility checking for Product / Patent 2) Poster draft1	
March 4 week	1)Draft Report1 and Poster draft2 submission 2) Final product demo to Guide	BE-8
March 4 week	Draft Report2 submission- Revised demo to guide	BE-8
April 1 week	Final Report submission and final poster	BE-8
April 1 week	Poster submission	BE-8
As per university schedule	Oral exam and TW Report evaluation	

Prof. Mahendra Mehra
Project In-charge

(Dr. B. S. Daga)
HOD

SAMPLE – ACADEMIC AUDIT (2019-2020)

Date: 03, July 2019

To,
The Principal,
FR.C.R.C.E., Bandra,Mumbai.

Subject: Request to sanction the honorarium for the member of Academic audit of Computer Department.

Dear Madam,

The department of Computer Engineering has rescheduled the Academic audit on 4th July 2019. So I request you to cancel the earlier approval to sanction the honorarium of Rs. 3000 and to consider the new revised remuneration of Rs. 5000 for the member mentioned below.

Sr. No.	Name of DAB Member	Designation	Amount
1	Dr. Abhijit Joshi	Associate Professor, Computer Department, D.J. Sanghavi College of Engineering, Mumbai	Rs.5000.00

Thanks and Regards,

(Prof. Sujata Deshmukh)
Coordinator, Computer Department.

2.1.1

Audit Observations by Dr. A.R. Joshi dated 04-07-19

1. The target level needs to be revised at program level for attainment. The data of previous year results should be used to set the new target level.
2. Quality of assessment should remain constant across all the assessment tools used for a particular course. It should be the policy of the department as the college is trying for autonomy.
3. Quality Paper publication should be increased.
4. Journals/conferences/ projects competitionparticipation of students and faculties require to be increased.
5. More innovative methods for teaching learning processing should be used
6. The awareness of the processes and its implementation must be rigorous.
7. Use of Moodle for teaching material

SOCIETY OF ST. FRANCIS XAVIER, PILAR'S

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

(Approved by AICTE & Affiliated to University of Mumbai)

Fr. Agnel Ashram, Bandstand, Bandra (W), Mumbai - 400 050.

Phone : (022) 6711 4000, 67114101, 6711 4104 • Fax : 6711 4100

Website : www.frcrce.ac.in • Email : crce@fragnel.edu.in

Ref.: CRCE / 2019

Date : July 4, 2019.

To,
Dr. Abhijit Joshi
Professor
D.J. Sanghvi College of Engg.
Mumbai

Sub.: Thanksgiving for being an Expert for Department Audit – Computer Engineering Dept.

Dear Sir,

We are very much thankful to you for conducting the Audit of the Computer Engineering Dept. of our College today, 4th July 2019 successfully and giving your valuable feedback.

Thanking you once again.

Yours faithfully,

(DR. SRIJA UNNIKRISHNAN)
PRINCIPAL

Received
4/7/19

Fr. Conceicao Rodrigues College of Engineering

Computer Engineering Department

Academic Audit Term 2019-2020

Name of the Faculty: Dr. Sunil Surve

Courses Taught: 1.(First Semester)Microprocessor

2. (Second Semester) Machine Learning

Sr.No.	Parameters to be verified	Very Good (4) Good(3) Adequate (2) Needs Improvement (1)	Remark
1	Lesson Plan and Execution	3	
2	Text and Reference	4	
3	Resource material available to students	3	
4	Rubrics Created and followed for assessment	3	
5	Mapping of COs with POs and PSOs	3	
6	Delivery Mechanism	3	
7	Content Beyond Syllabus	4	
8	Quality of UT Question Paper	4	
9	Quality of Lab Manual	—	
10	Students Performance evaluation methods, analysis of assessment results and corrective measures.	5	
11	Methods adopted for improving performance of weak students	3	
12	Help rendered to students w.r.t. career/skill development	✓	
13	Projects Guided	✓	
14	Any administrative responsibility handled	✓	

Audited By : Dr. A. R. JOSHI

Sign : 4/7/19

PART B

Criterion 1 – Curricular Aspects

Key Indicator – 1.1 Curricular Planning and Implementation

1.1.2 - SUPPORTING DOCUMENTS

FR. Conceicao Rodrigues College of Engineering

1.1.2 Supporting Documents

SAMPLE- CIRCULAR EXECUTIVE COMMITTEE MEETING

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Fr. Agnel Ashram, Bandstand, Bandra (West), Mumbai – 400 050.

Ref.: CRCE / 2019 / 424

Date : October 14, 2019.

NOTICE

To,
The Executive Committee Members

A meeting of the Executive Committee is scheduled on Wednesday, 16th October 2019 at 10.30 AM in the Conference Room (Fifth Floor) to discuss the following matters.

AGENDA

1. Academic Matters
2. Readiness for NAAC Visit

Any other matter with the permission of the Chair.

All the members are requested to attend.

(DR. SRIJA UNNIKRISHNAN)
PRINCIPAL

1. Dr. V.S. Jorapur, HOD – Production Engg.
2. Dr. Sapna Prabhu, HOD – Electronics Engg.
3. Dr. B.S. Daga, HOD – Computer Engg.
4. Dr. Jagruti Save, HOD – Info. Tech.
5. Dr. Hemant Khanolkar, HOD – Hum. & Sci.
6. Dr. S.K. Surve, Dean – Academics
7. Dr. D.V. Bhoir, Dean – Students Affairs
8. Dr. Bhushan Patil, Dean – Research & Development
9. Dr. V.S. Bilolikar, Examination Cell Incharge
8. Mr. Mahesh Sharma, Training & Placement Officer
10. Mr. Chandrashekhar Shetty, Registrar

SAMPLE- MINUTES EXECUTIVE COMMITTEE MEETING

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING

Fr. Agnel Ashram, Bandstand, Bandra (W), Mumbai – 400 050.

MINUTES OF THE EXECUTIVE COMMITTEE MEETING HELD ON 20TH JULY 2019 IN THE CONFERENCE ROOM (FIFTH FLOOR) AT 10.00 AM

MEMBERS PRESENT:

1. Dr. Srija Unnikrishnan (In the Chair)
2. Dr. V.S. Jorapur
3. Dr. Sapna Prabhu
4. Dr. B.S. Daga
5. Dr. Jagruti Save
6. Dr. Hemant Khanolkar
7. Dr. D.V. Bhoir
8. Dr. S.K. Surve
9. Dr. Bhushan Patil
10. Mr. Mahesh Sharma

Principal welcomed the members.

Principal briefed members that the main agenda of the meeting is to take follow-up on the agenda items discussed in the previous HODs and Deans meeting held on 29th June 2019.

The following discussions were held:

Item No.1: Project based learning

Principal told members to implement Project based learning at all levels possible – individual subjects, Mini Projects, Dept. wise projects. She said that the objective behind the concept of project based learning it is to engage or get maximum students involved in Projects, thereby enhancing their learning and placement prospects.

Dr. Sapna Prabhu commented that through Project Cell, some projects have been initiated for the E-Yantra competition. Groups of 4 students each from SE & TE classes have been formed and they are assigned the mentors.

Dr. Jagruti Save, informed that many mini-projects are going on in the IT Dept. The third year students are engaged in 4 hours separate project which was started during their second year. Under this project, students have developed 2 modules for website which can facilitate easy data collection. The project is still going on. The problem statement for second Year students is yet to be given. Many students are doing NPTEL courses and internships.

Item No.2: Innovative experiment for each lab. course

For every lab course, each student group can design and implement one innovative experiment, related to the subject. The respective faculty can guide the students. The best innovative experiment subjectwise / yearwise / department wise can be given recognition.

Item No.3: Academic Monitoring

- HODs will follow up the Lesson plan, Tutorial/Practical plan submitted by faculty.

...2/-

- Principal apprised members about the change in FE term commencement date, as the CAP round reporting has been extended. Induction Programme, spread across the year, should be held as specified by the University. Institute should award certificates to all students on successful completion of the Induction Programme, based on their report and presentation. Dr. Hemant Khanolkar read out the schedule of the Induction Programme. Principal told Dr. Khanolkar to prepare an action plan, work out the logistics and keep records of the programmes for issue of certificates.
- Dr. Khanolkar informed that FE Results have been declared and the overall passing percentage of students is 74%. He read out subjectwise and branchwise passing percentages. Student from Production Engg. branch, Mr. Amit Dubey, stood overall first.
- It was decided to hold FE faculty meeting on the coming Monday. Chapter wise notes are to be prepared by faculty for first year students. Hard copy as well as soft copy of the notes can be given to first year students.
- Principal told that faculty members should start doing attendance entries from 19nd July 2019.

Item No.4: Effective use of laboratory slots

- Principal expressed concern that the Lab sessions are not effectively utilised. Placement companies had mentioned about the poor Practical knowledge and experience of students. The tendency of copying/downloading codes/expt. design should be curtailed. Teachers should give multiple and challenging problems to students in the same batch, so that students find solutions on their own. If required, internet can be disabled during specific lab sessions.
- HODs can identify good departmental projects which can be preserved and students re-imbursed, with proper bills. Project competitions can be held department-wise.

There was no other item for discussion.

Principal thanked members for attending the meeting and their active participation.

(Dr. SRIJA UNNIKRISHNAN)
PRINCIPAL

Copy to:

1. Rev. Fr. Peter D'Souza, Local Superior – for information
2. Rev. Fr. Valerian D'Souza, Director – for information
3. Dr. V.S. Jorapur 4. Dr. Sapna Prabhu 5. Dr. B.S. Daga
6. Dr.. Jagruti Save 7. Dr. Hemant Khanolkar 8. Dr. D.V. Bhoir
9. Dr. S.K. Surve 10. Dr. Bhushan Patil 11. Dr. V.S. Bilolikar
12. Mr. Mahesh Sharma 13. Mr. C.B. Shetty

SAMPLE- INSTITUTE ACADEMIC CALENDAR

ODD SEMESTER (2019-2020)

ACADEMIC CALENDAR (2019-2020) -ODD SEMESTER

Month	Holidays	Extra/Co-curricular Events	Curriculum Plan	Staff Notice
July		July 3-13 - Football Tournment	July 1 - College reopens (SE, TE, BE)	July 5 - Faculty Meeting
Su M Tu W Th F Sa				
1 2 3 4 5 6				
7 8 9 10 11 12 13				
14 15 16 17 18 19 20				
21 22 23 24 25 26 27				
28 29 30 31				
August				
Su M Tu W Th F Sa				
1 2 3	Aug 12 - Bakri Id	Aug 23 - Synergy	August 7 - FE opens	QP and Model Answer upload for Unit
4 5 6 7 8 9 10	Aug 15 - Independence Day			Test 1 (SE, TE, BE) : Link active between Aug 1-3
11 12 13 14 15 16 17	Aug 17 - Parsi New Year		Aug 13, 14 & 16 - Test 1 (SE, TE, BE)	Unit test 1 marks entry : Link active
18 19 20 21 22 23 24			August 18-13 - Mid Term Feedback (SE, TE, BE)	between Aug 18-20
25 26 27 28 29 30 31			August 19-23 - Induction Program	
September				
Su M Tu W Th F Sa				
1 2 3 4 5 6 7	Sept 2-6 - Mid Term Break	Sept 13-14 - TeDx Saloni	Sept 11-13 - Mid Term Feedback (FE)	
8 9 10 11 12 13 14	Sept 10 - Moharum	Sept 27-28 - CRMD		
15 16 17 18 19 20 21				
22 23 24 25 26 27 28				
29 30				
October				
Su M Tu W Th F Sa				
1 2 3 4 5	Oct 2 - Mahatma Gandhi Jayanti		Oct 14-16 - Test (FE, SE, TE, BE)	
6 7 8 9 10 11 12	Oct 8 - Dasara		Oct 18 - Submission (SE, TE, BE)	QP and Model Answer upload for Unit Test (FE, SE, TE, BE): Link active between Oct 3-5
13 14 15 16 17 18 19	Oct 27 - Laxmi Poojan		Oct 14-18 -Feedback (SE, TE, BE)	Unit test 2 marks entry : Link active
20 21 22 23 24 25 26	Oct 28 - Diwali		Oct 18 - Defaulter List	between Oct 16-18
27 28 29 30 31	Oct 29 - Bhaubeej		Oct 18 - Term Ends (SE, TE, BE)	
November				
Su M Tu W Th F Sa				
1 2	Nov 10 - Id-E-Milad		Nov 4-8 - Prelims - Test 2 (FE)	QP and Model Answer upload for Unit
3 4 5 6 7 8 9	Nov 12 - Guru Nanak Jayanti		Nov 11 - Submission (FE)	Test 2 (FE) : Link active between Oct 30-Nov 1
10 11 12 13 14 15 16			Nov 1-11 -Feedback (FE)	Unit test 2 marks entry : Link active
17 18 19 20 21 22 23			Nov 15 - Defaulter List	between Nov 11-14
24 25 26 27 28 29 30			Nov 16 - Term Ends (FE & ME)	
December				
Su M Tu W Th F Sa				
1 2 3 4 5 6 7	Dec 25 - Christmas			
8 9 10 11 12 13 14				
15 16 17 18 19 20 21				
22 23 24 25 26 27 28				
29 30 31				

SAMPLE- INSTITUTE ACADEMIC CALENDAR

EVEN SEMESTER (2019-2020)

Month	Holidays	Extra/Co-curricular Events	Curriculum Plan	Staff Notice
January 2020				
S M T W T F S				
1 2 3 4		Jan 18-26 - Athlos		
5 6 7 8 9 10 11			Jan 6 - College Reopens	Jan 14 - Faculty Meeting
12 13 14 15 16 17 18				
19 20 21 22 23 24 25				
26 27 28 29 30 31	26 Jan - Republic Day			
February 2020				
S M T W T F S				
1	19 Feb – Chhatrapati Shivaji Maharaj Jayanti	Feb 1 - Sports Day		
2 3 4 5 6 7 8		Feb 15 - Convocation		
9 10 11 12 13 14 15		Feb 17, 18, 20 - Euphoria	Feb 26-28 - First Unit Test	QP and Model Answer upload for Unit Test 1: Link active between Feb 15 - 22
16 17 18 19 20 21 22				
23 24 25 26 27 28 29	21 Feb - Mahashivratri			
March 2020				
S M T W T F S			Mar 2-6 -Mid-term Feedback	
1 2 3 4 5 6 7				Marks entry for Unit Test 1: Link Active between Feb 28 - Mar 7
8 9 10 11 12 13 14	10 Mar - Holi			
15 16 17 18 19 20 21		Mar 20-21 - Crescendo		
22 23 24 25 26 27 28	25 Mar - GudiPadva			
29 30 31				
April 2020				
S M T W T F S			Apr 1-13 - Feedback	QP and Model Answer upload for Unit Test 1
1 2 3 4	Apr 6 - MahavirJayanti		Apr 7-9 - Second Unit Test	Link active between Mar 30 - Apr 2
5 6 7 8 9 10 11	Apr 10 - Good Friday	Apr 4 - TedX Main Event	Apr 17 – TW Submission	
12 13 14 15 16 17 18	Apr 14 - Dr.Babasaheb Ambedkar Jayanti		Apr 18 - Defaulter List	Marks entry for Unit Test 1:
19 20 21 22 23 24 25			Apr 18 - Term Ends	Link Active between Apr 9 - 15
26 27 28 29 30			Apr 20-30 – Oral/ Practical Exam	
May 2020				
S M T W T F S				
1 2	May 1 - Maharashtra Din		May 7-25 – Theory Examination (Regular)	
3 4 5 6 7 8 9	May 7 - Buddha Pournima			
10 11 12 13 14 15 16			May 26-June 11 – Theory Examination (ATKT)	
17 18 19 20 21 22 23				
24 25 26 27 28 29 30	May 25 - Ramzan Id			
31				
June 2020				
S M T W T F S				
1 2 3 4 5 6				
7 8 9 10 11 12 13				
14 15 16 17 18 19 20				
21 22 23 24 25 26 27				
28 29 30				

Commencement of Next Term 6th July 2020

Dr. Srija Unnikrishnan

Principal

SAMPLE- DEPARTMENT ACDEMIC CALENDAR

ODD SEMESTER (2019-2020)

DEPARTMENT OF COMPUTER ENGINEERING
ACADEMIC CALENDAR
2019-2020

Dates	Curriculum Plan	Staff Notice	Extra/Co-curricularEvents	Student Bodies
Jul 1	College reopens (SE-BE)			
Jul 3-13			Intra-college Foot ball	
Jul 3	BE Students Project Abstract submisssion (till 3 July)	Faculty Project Proposal Idea Submission (till 3 July)		
Jul 5		Faculty meeting (college level)		
Jul 6		Departmental Faculty meeting		
Jul 8		Project topic approval Presentation		
Jul 15		Lesson Plan with Lecture/Lab/ Assignment/Mini Projects Plan Submission PAC		
Jul 15		Lab Manual Submission		
Jul 15		SE-TE Mentors List		
Jul 24		Allocation of BE Project Guides		
Jul 30		UT1 Paper Submission to PAC		
Aug 02		PAC Meeting (Assessment of CO, CO-PO mapping, lesson Plan)		
		Final project problem definition with guide(with research Papers)		
Aug 1-3		UT1 Question paper and model answer upload SE-BE (Link active Aug 1-3)		
Aug 3				Mozilla : NodeJS and MongoDB workshop
Aug 10				CodeLabs:Algoholic 1.0
Aug 13,	Unit Test 1			
Aug 19-21		UT1 Marks entry, UT1 Result analysis, List of weak students. (Aug 19-21)		
Aug 19-21	Mid Term Feedback			
Aug 20				CodeLabs:Introduction to Python and Machine learning
Aug 23			Synergy	CSI Event 1, CodeLabs:Algoholic 2.0, PUBG/Bombsquad
Aug24-Aug25			Badminton (Aug 25)	CodeLabs: Practical approach to Machine Learning
Aug 26		**Mid term Presentation1** with research Papers and work attempted 40%		
Aug 31				IOT workshop
Sept 2-6			Mid Term Break	Mozilla:Ethical Hacking Seminar,
Sept 7				
Sep 23		**Mid term Presentation2** with work attempted 80%		CodeLabs: Quiz on OOPM
Sept 27-		TE PBL Progress Report	CRMD	
Oct 1		UT2 Paper Submission to PAC , PAC Meeting		
Oct 3-5		UT2 Question paper and model answer upload (Link active Oct 3-5)		Mozilla: 05 Oct Github Workshop
Oct 14 -	Unit Test 2			
Oct 7-18	Final Feedback			
Oct 7		BE Project Report submission and 100% work done		
Oct 1 -4		Remedial Classes		
Oct 17-22		UT2 Marks entry (Link active Oct 17-22)		
Oct 18	Term Work Submission			
Oct 18	Defaulters list			
Oct 18		CO Attainment without results		
Oct 18	Term End (SE TE BE)			
Oct 21		Department Faculty Meeting		
AS per University	Practical and Oral Exams	BE Project SEM VII Final Examination		

SAMPLE- DEPARTMENT ACDEMIC CALENDAR

EVEN SEMESTER (2019-2020)

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING, BANDRA

ACADEMIC PLANNER : JANUARY-MAY 2019

Dates	Extra/Co-curricular Events	Curriculum Plan	Staff Notice	Student Bodies
Jan-01		College Reopens (for SE, TE & BE)		
Jan-05	Alumni Meet			
Jan-08		Faculty meeting		
Jan-08			Book Recommendations to central and departmental library	
Jan-16			Lesson Plan Submission to PAC	
Jan 18-25	Athlos		Lab Manual/Quiz submission	
Jan-18			Assignment formulation (1st and 2nd) with	
Jan-21			PAC Meeting, QP1/Assignments Submission	
Jan21-25			QP and Model Answer upload for Unit test 1 : Link active between Jan 21 - Jan 25	
Jan-28			First mid term presentation(project)	
Jan-29				FE Coding Contest: Codelabs
Jan-31	Annual Sports day		Faculty Meeting(departmental)	
Feb-02			Follow up of defaulters' student by class teacher	
Feb 4,5,6		Unit Test 1 (FE,SE,TE,BE)		
Feb 6-12			UT 1 marks entry : Link active between Feb 6-12	
Feb-09				HTML and CSS workshop: MozillaCRCE
Feb 13-15	Euphoria			
Feb-18			Assignment 1 Evaluation (Tentative)	
Feb 18-22		Mid Term Feedback		
Feb-23	Convocation			
Feb-26			Follow up of defaulters' student by class teacher	
Feb-27			Assignment 2 Evaluation (Tentative)	
Mar 2-3	Intercollegiate Hackathon			
Mar-09				Mozi Talk MozillaCRCE
Mar 15-16	Crescendo			Capture the flag(debugging), Image Capture: MozillaCRCE Counter Strike, Code Swapping:CSI Algoholic 4.0, Treasure Hunt : Codelabs
Mar-22			PAC meeting	
Mar-25			Internal BE Project presentation: 2nd stage	
Mar 25-29			QP and Model Answer upload for Unit test 2 : Link active between March 25-29	
Mar 30-31				Unscript Hackathon:MozillaCRCE, CodeLabs
Apr-02			Follow up of defaulters' student by class teacher	
April 8,9,10		Unit Test 2 (SE, TE, BE)		
April 8-12		FE Prelims		
April 8-16		Final FB (FE,SE,TE,BE)		
April 10-15			UT 2 marks entry : Link active between April 10-15	
Apr-15		Term WorkSubmission		
Apr-09			Internal BE Project Presentation: Final stage	
Apr-02			Submission of soft copy of Black Book: a. rough draft	
Apr-12			b. revised draft	
Apr-16			C. Final draft	
Apr-18			Defaulter List	
Apr-20		Term End		
Apr-22			Termwork Sheet, Grading Sheet	
Apr 22-27			April External oral exam (Project)	
April 22 onwards		External Practical + Oral Exams		
May-03			CO Attainment Submission (Current Sem without results)	
May-04			SAR Related work	
May- June			DAB Meeting, Academic Audit	

Dr. B.S. Daga

Head,
Department of Computer Engineering

SAMPLE- CO ATTAINMENT CALCULATION

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**
CSC302.1 : Perform number system and code conversions **Target : 2.5**

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
TEST	0.2	No. of students scoring >= 4.8 out of 8 in Q-1 (T1)	60	84.51	3	0.6
60% students will score minimum 60% marks						
MODULE TEST1	0.2	No. of students scoring >=14 out of 20 in ass1	47	71.21	1	0.2
70% students will score minimum 70% marks						
QUIZ	0.2	No. of students scoring >=14 out of 20 in Quiz1	58	81.69	2	0.4
65% students will score minimum 70% marks						
UNI THEORY	0.2	No. of students acoring >= 48 out of 80	50	70.42	2	0.40
60% students will score minimum 60% marks						
UNI PRACTICAL	0.2	No. of students acoring >= 17.5 out of 25	70	98.59	3	0.6
60% students will score minimum 70% marks						
INDIRECT METHOD						**2.2**
Course Exit Survey	1	No. of students agree + strongly agree	65	1	3	3
75% students will score minimum 75% marks		No. of respondents = 65				
No. of students	**71**					

Levels	Test	QUIZ	Module Test	End sem exam(TH)	End sem exam(PR)	Survey
1 (Low)	60-69	65-74	70-79	60-69	60-69	75-80
2 (Medium)	70-79	75-84	80-89	70-79	70-79	81-85
3 (High)	80 and above	85 and above	90 and above	80 and above	80 and above	86 above

CO1 Attainment = 2.36

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**
CSC302.2: Design combinational circuits **Target : 2.5**

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
TEST (T1+T2)	0.2	No. of students scoring >= 10.8 out of 18 in Q-2(8)+Q-3(4) in T1 & Q-1 (6M) T2	47	66.20	1	0.2
60% students will score minimum 60% marks						
LAB	0.2	No. of students scoring >=56 out of 80 in exp1-7,11	70	98.59	3	0.6
70% students will score minimum 70% marks						
ASSIGNMENT	0.2	No. of students scoring >=14 out of 20 in Quiz1	69	97.18	3	0.6
60% students will score minimum 70% marks						
UNI THEORY	0.2	No. of students acoring >= 48 out of 80	50	70.42	2	0.4
60% students will score minimum 60% marks						
UNI PRACTICAL	0.2	No. of students acoring >= 17.5 out of 25	70	98.59	3	0.6
60% students will score minimum 70% marks						
INDIRECT METHOD						**2.4**
Course Exit Survey	1	No. of students agree + strongly agree	65	1	3	3
75% students will score minimum 75% marks		No. of respondents = 65				
No. of students	**71**					

Levels	Test	ASSIGNMENT	LAB	End sem exam(TH)	End sem exam(PR)	Survey
1 (Low)	60-69	60-69	70-79	60-69	60-69	75-80
2 (Medium)	70-79	70-79	80-89	70-79	70-79	81-85
3 (High)	80 and above	80 and above	90 & above	80 and above	80 and above	86 above

CO2 Attainment = 2.52

SAMPLE- CO ATTAINMENT CALCULATION

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**

CSC302.3 : Design sequential circuits. **Target : 2.5**

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
TEST (T2)	0.2	No. of students scoring >= 9 out of 14 in Q2(6) + Q3(8) in T2	31	43.66	0	0
60% students will score minimum 60% marks						
LAB	0.2	No. of students scoring >=28 out of 40 in exp8,9,10,12	70	98.59	3	0.6
70% students will score minimum 70% marks						
MODULE TEST2	0.2	No. of students scoring >=14 out of 20 in Quiz1	57	80.28	3	0.6
60% students will score minimum 70% marks						
UNI THEORY	0.2	No. of students acoring >= 48 out of 80	50	70.42	2	0.4
60% students will score minimum 60% marks						
UNI PRACTICAL	0.2	No. of students acoring >= 17.5 out of 25	70	98.59	3	0.6
60% students will score minimum 70% marks						
INDIRECT METHOD						2.2
Course Exit Survey	1	No. of students agree + strongly agree	65	1	3	3
75% students will score minimum 75% marks		No. of respondents = 65				
No. of students	**71**					

Levels	Test	Module Test	LAB	End sem exam(TH)	End sem exam(PR)	Survey
1 (Low)	60-69	60-69	70-79	60-69	60-69	75-80
2 (Medium)	70-79	70-79	80-89	70-79	70-79	81-85
3 (High)	80 and above	80 and above	90 & above	80 and above	80 and above	86 above

CO3 Attainment = 2.36

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**

CSC302.4: Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design
Target : 2.5

Assessment Tools	Weightage	NO. of successful students		Percentage	Level	Attainment
DIRECT METHODS						
LAB	0.2	No. Of students scoring 14 or more out of 20 in EXP 11,12	71	1.00	3	0.6
70% students will score minimum 70% marks						
MINI PROJECT	0.8					
65% students will score minimum **70%** marks		No. of students score 10.5 or more out of 15 =	71	1.00	3	2.4
						3
INDIRECT METHOD						
Course Exit Survey	1	No. of students agree + strongly agree	64	0.98	3	3
		No. of respondents = 65				

Level	Lab	Mini Project
1	70-79	65-74
2	80-89	75-84
3	90 & above	85 and above

CSC302.4 Attainment = 3

SAMPLE- PO ATTAINMENT CALCULATION

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering
SUBJECT: Digital Logic Design & Analysis (CSC302)
BRANCH/SEMESTER: COMPUTER /III **Academic Year: 2019-20**

CO	Description	Attainment
CSC302.1	Perform number system and code conversions	2.36
CSC302.2	Design combinational circuits	2.52
CSC302.3	Design Sequential circuits	2.36
CSC302.4	Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design	3

PO Attainment

CO Number	Course Outcome	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	CO Attain
CSC302.1	Perform number system and code conversions	3												3		2.36
CSC302.2	Design combinational circuits.	3	2	3	1									2		2.52
CSC302.3	Design sequential circuits.	3	2	3	1									3		2.36
CSC302.4	Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design	3	3	3	3					2	2			3		3
Total		12	7	9	5					2	2			11		
CO-PO MATRIX		3	2.33	3.00	1.67					2	2			2.75		
PO ATTAINMENT		1.92	2.77	2.6	2.86					3	3			2.55		

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

BE - PROJECTS - PLAN

Fr. Conceicao Rodrigues College of Engineering

Department of Computer Engineering

2019-2020

Project Activity Schedule

B.E Computer Engineering

Date/week	Activity	Class
First week of May/End of April	Project Idea Submission Notice for Students and faculty Period for idea submission- Till 3July 2019	TE -6
BE-7 Activities		
July 1/2 week (08/072019)	Project topic approval Presentation	BE-7
July 3 / 4 week (24/07/2019)	Assigning guides to Project	
August1/2 week (Till 03/08/2019)	Final project problem definition with guide(with research Papers)- Assigning new topics to Rejected project topic based on project idea submitted by faculties/ revision of Problem definition	
September 2/3 week (11/09/2019)	**Mid term Presentation1** with research Papers and work attempted 40%	BE-7
October 1/2 week (05/10/2019)	**Mid term Presentation2** with work attempted 80%	BE-7
October 2/3week	Report submission and 100% work done	BE-7
As per university schedule	Oral exam and TW report evaluation	BE-7
BE-8 Activities		
February 1 / 2 week (10/02/2020)	**Mid term Presentation1**- 1)Rough draft1 of research paper 2)Product features specifications with market research 3) Abstract submission to conferences or Journals	BE-8
March 1 / 2 week	**Mid term Presentation2** - 1)Final draft2 of research paper 2)Product features Implementation 3) Final paper submission to conferences or Journals	BE-8
March 3 / 4week	1)Implementation /demo to guide- Possibility checking for Product / Patent 2) Poster draft1	
March 4 week	1)Draft Report1 and Poster draft2 submission 2) Final product demo to Guide	BE-8
March 4 week	Draft Report2 submission- Revised demo to guide	BE-8
April 1 week	Final Report submission and final poster	BE-8
April 1 week	Poster submission	BE-8
As per university schedule	Oral exam and TW Report evaluation	

Prof. Mahendra Mehra
Project In-charge

(Dr. B. S. Daga)
HOD

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 1 : ODD SEM (2019-2020)

FACULTY CIRCULAR

Fr. Conceicao Rodrigues College of Engineering

Department of Computer Engineering

B.E Computer Engineering **Academic year: 2019-20**

Date: 22- 08- 2019

CIRCULAR

All faculties of Computer engineering department are here by informed that **First internal mid-term project presentation** for **Major Project 1** is scheduled on **Wednesday, 11th September 2019.** Students are required to present detailed analysis, design, architecture of the proposed system and work done so far along with the timeline.

An Excel sheet has been shared on official E-mail ids, Kindly update the BE Project titles of your respective Groups.

Schedule for the presentation will be informed on 26th August 2019.

Dr. B.S. Daga
H.O.D
(Computer Engineering Department)

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 1 : ODD SEM (2019-2020)

STUDENT CIRCULAR

Fr. Conceicao Rodrigues College of Engineering

Department of Computer Engineering

B.E Computer Engineering **Academic year: 2019-20**

Date: 22- 08- 2019

NOTICE : Major Project1- First Mid Term Presentation

BE STUDENTS

All students of B.E Computer engineering are hereby informed that **Midterm presentation-1 of Final year Project has been scheduled on Wednesday, 11th September 2019, at 10:00am onwards.** The detail schedule will be displayed on 26th August 2019. All students are required to meet Projects Guides weekly, and shows the project progress also finalize the project title which cannot be changed later.

Presentation must include following details of proposed Project:

- Introduction
- Literature review
  - Background
  - Literature Review (with citations)
  - Summary of literature
  - Research Gap
- Motivation
- Problem statement
- Objectives
- Scope / significance/relevance of System
- Applications and Existing system
- Proposed Architecture of system
- Methodology
  - Algorithms / Technologies /software specifications
  - Hardware specification
- References (IEEE format)

NOTE: Pl. Bring hard copy of Main research Paper without fail and keep soft copy of all related Research papers in one folder.

Prof. Mahendra Mehra
(Project coordinator)

Dr. B.S. Daga
H.O.D
(Computer Engineering Department)

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 1 : ODD SEM (2019-2020)

Fr. Conceicao Rodrigues College of Engineering
Department of Computer Engineering
B.E. Major Project 1 FIRST MIDTERM PRESENTATION VENUE AND PANEL DETAILS
Date : 11/09/2019 **Time:10:00am onwards**

PANEL 1: Prof Swati & Prof Roshini					
Group No.	**Roll No**	**Name of Student**	**Project Title**	**Guide Name**	**venue**
1	7968	Cajetan Rodrigues	Voice Enabled AI-based Drone for Shipping and Delivery.	Prof. Ringe Swati	LAB NO 703 10:00AM onwards
	7973	Vedant Sakhardande			
	7918	Atharva Atre			
2	7949	Sharwari Marathe	Web Semantics		
	8169	Rajesh Manjrekar			
	8171	Raksha Shetty			
3	7966	Shreya Raut	Pimple detector and solution provider	Prof. Padate Roshni	
	7967	Renita Augustin			
	7946	Hazel Lobo			
4	7921	Dhananjay Chobhe	Fire Detection and Extinguishment System		
	7962	Davina Pinto			
		Aniket Tari			

Fr. Conceicao Rodrigues College of Engineering
Department of Computer Engineering
B.E. Major Project 1 FIRST MIDTERM PRESENTATION VENUE AND PANEL DETAILS
Date : 11/09/2019 **Time:10:00am onwards**

PANEL 2: Dr. Daga & Prof Kalpana					
Group No.	**Roll No**	**Name of Student**	**Project Title**	**Guide Name**	**venue**
5	7916	Aishwarya Sebin	Speech Assistance for the Deaf	Prof. Deorukhkar Kalpana	LAB NO 710 10:00AM onwards
	7941	Gauri Jare			
	7972	Wencita Rodrigues			
6	7979	Deljin Jaison	Text summarisation		
	7940	Sanjeev H.			
	8124	Shubham Ambilkar			
7	7922	Rochelle Cordeiro	Candidate interview evaluation	Dr. Daga B. S.	
	7933	Brinel Dsouza			
	7978	Anol Kurian			
8	7965	Karan Rao	Visual simultaneous localisation and mapping		
	7917	Christo Aluckal			
	7627	Sumedh Deshpande			
9	7920	Juhi Checker	Job Role Prediction		
	7926	Sayali Deo			
	8160	Anne Rajan			

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 1 : ODD SEM (2019-2020)

Fr. Conceicao Rodrigues College of Engineering
Department of Computer Engineering
B.E. Major Project 1 FIRST MIDTERM PRESENTATION VENUE AND PANEL DETAILS
Date : 11/09/2019 **Time:10:00am onwards**

PANEL 3: Dr. Sujata & Prof Merly					
Group No.	**Roll No**	**Name of Student**	**Project Title**	**Guide Name**	**venue**
10	7944	Kartick Hariharan	AI-based GIS Mapping for Effective Disaster Relief and Recovery Operations	Dr. Deshmukh Sujata Prashant	LAB NO 704 10:00AM onwards
	7945	Ashley Lobo			
	7947	Shawn Lopes			
11	8167	Chinmay Gaonkar	Neural Voice Cloning		
	8162	Sumedh Bhatkar			
	8170	Prerna Pallan			
12	7942	Jerome Nicholas	Lip reading App for the deaf/dumb and also for	Prof. Thomas Merly	
	7936	Kenrick Fernandes			
13	7961	Nerissa Pereira	Diagnosis of Heart Disease using Adaptive Network- Based Fuzzy Interference		
	7923	Simran Dabreo			
	7971	Linnet Rodrigues			

Fr. Conceicao Rodrigues College of Engineering
Department of Computer Engineering
B.E. Major Project 1 FIRST MIDTERM PRESENTATION VENUE AND PANEL DETAILS
Date : 11/09/2019 **Time:10:00am onwards**

PANEL 4: Dr. Surve & Prof Supriya					
Group No.	**Roll No**	**Name of Student**	**Project Title**	**Guide Name**	**venue**
14	7977	Yash Turkar	Indoor Navigation system using RGB-D Imaging	Dr. Surve Sunil	LAB NO 604 10:00AM onwards
	7928	Yashom Dighe			
15	7975	Manish Singh	Mutual Fund Suggestions App		
	7932	Sunny Dodhiya			
16	8164	Glen Dabre	Smart Exercise Monitoring System	Prof. Kamoji Supriya	
	8163	Chris Carvalho			
	7970	Lenis Rodrigues			
17	7931	Alphaeus Demonte	Vehicle Tracking		
	7938	Solomon Jose			
	7960	Clayton Pereira			

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 1 : ODD SEM (2019-2020)

Fr. Conceicao Rodrigues College of Engineering
Department of Computer Engineering
B.E. Major Project 1 FIRST MIDTERM PRESENTATION VENUE AND PANEL DETAILS
Date : 11/09/2019 **Time:10:00am onwards**

PANEL 5: Prof Sunil & Prof Dipali					
Group No.	**Roll No**	**Name of Student**	**Project Title**	**Guide Name**	**venue**
18	7924	Lenson Daniel	Music generation using Neural Network	Prof. Chaudhari Sunil	LAB NO 611 10:00AM onwards
	7958	Aditya Patil			
	7952	Alex Saji			
19	7951	Aakash Mishra	IOT system for tyre safety		
	8125	Sarvesh Gupta			
	7954	Prabhu Anand			
20	7919	Shreya Bhujbal	AI for Crime Prevention	Prof. Koshti Dipali	
	7943	Nehal Kalnad			
	7976	Suyash Sreekumar			
21	7957	Chinmay Paralkar	Sales Forecast App		
	8126	Kajal Sapkal			
	7963	Royston Pinto			

Fr. Conceicao Rodrigues College of Engineering
Department of Computer Engineering
B.E. Major Project 1 FIRST MIDTERM PRESENTATION VENUE AND PANEL DETAILS
Date : 11/09/2019 **Time:10:00am onwards**

PANEL 6: Prof. Ashwini, Prof. Monali & Prof Mahendra					
Group No.	**Roll No**	**Name of Student**	**Project Title**	**Guide Name**	**venue**
22	7937	Simran Gadkari	Diabetic Retinopathy Detection	Prof. Pansare Ashwini	LAB NO 609 10:00AM onwards
	7950	Jenell Mathias			
	7959	Merlin Payapilly			
23	7935	Leon Falcao	Topic to be confirmed with guide consultation		
	7929	Macwill Dmello			
	7969	Kevin Rodrigues			
24	7925	Steve D'Costa	Topic to be confirmed with guide consultation	Prof. Mehra Mahendra	
	7930	Ryan D'Mello			
	7955	Joseph George			
25	7953	Sohaa Mutsaddi	An AI based chatbot for medical assistance		
	7948	Shubham Mankar			
26	7956	Chaitanya	Success prediction of films at box office using ml	Prof. Shetty Monali	
	7974	Suyash			
	7964	Sankalp			
27	8168	Ofrin Lopes	Android app name : Total Guide		
	8161	Manthan Bhatkar			
	8165	Christina Daniel			

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 1 : EVALUATION SHEET FORMAT

Fr. Conceicao Rodrigues College of Engineering
Department of Computer Engineering

First Mid Term Presentation Evaluation Sheet
Academic year 2019-20

Class/Sem-B.E/SEM VII **Venue:**
Presentation Date: 11th September 2019 **Project Guide:**

Course outcomes Assessed:

CO1: Practice the process of software project development in delivering successful IT projects.

CO2: Identify, summarize and analyze an appropriate literature and relate them to the problem in hand.

CO3: Design a solution to chosen problem using appropriate approach or methodology considering professional ethics and responsibility towards societal, Health, safety and legal issues.

DELIVERABLES →		Clear understanding of goals and objectives (CO1)	Identification of constraints (CO1)	SRS document (CO1)	Identification of relevant Literature (CO2)	Summarization of results and findings of the overall literature review process (CO2)	Identification of project phases (CO3)	Identification of tools and Technologies to be used (CO3)	Identification of possible Problems at each stage and suggestion on prevention methods (CO3)	Total
MARKS DISTRIBUTION→		4M	4M	8M	6M	6M	10M	6M	6M	50M
Roll no	**Student Name**	**Project Title:**								

Panel members:

Sign			
Name			

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 2 : ODD SEM (2019-2020)

FACULTY CIRCULAR

Fr. Conceicao Rodrigues College of Engineering

Department of Computer Engineering

B.E Computer Engineering **Academic year: 2019-20**

Date: 25- 09- 2019

CIRCULAR

All faculties of Computer engineering department are here by informed that **Second internal mid-term project presentation** for **Major Project 1** is scheduled on **Saturday, 05th October 2019**. Students are required to present Literature review, Architecture of the proposed solution and Implementation done so far along with the timeline.

Project guides are required to go through the title approval sheet which is attached along this circular and mark any discrepancies on the paper and sign the same also make a note of the students who attended the **"Understanding software design workshop"** on 23rd September 2019 for the groups under you.

Schedule of the presentation will be informed on 3rd October 2019.

Dr. B.S. Daga
H.O.D
(Computer Engineering Department)

SAMPLE – FINAL YEAR PROJECT ASSESSMENT

MID-TERM PRESENTATION 2 : ODD SEM (2019-2020)

STUDENT CIRCULAR

Fr. CRCE e-mail

swati CRCE <swati@fragnel.edu.in>

Circular : BE Major Project 1- First Midterm Presentation (2nd-7th November 2020)
1 message

Mahendra Mehra CRCE <mahendra.mehra@fragnel.edu.in> Mon, Oct 26, 2020 at 2:13 PM
To: Computer Department <comp@fragnel.edu.in>

Dear All,
All faculties of the Computer Engineering department are hereby informed that the BE Computers, Major Project I, First Midterm Presentations are scheduled from 2nd November to 7th November 2020. A Judges panel consisting of two guides have been formed who will be evaluating the Project Progress. The guides in the panel will have to communicate with one another and fix a suitable date and time on or before 2nd November 2020 and convey the same to their project groups. Judges panel and teams list is attached below.

Students have been asked to prepare PPT consisting of following slides in the order given:

- Introduction
- Literature review
  - Background
  - Literature Review (with citations)
  - Summary of literature
  - Research Gap
- Problem statement
- Objectives
- Scope / significance/relevance of System
- Applications and Existing system
- Proposed Architecture of system
- Methodology
  - Algorithms / Technologies /software specifications
  - Hardware specification
- References (IEEE format)

Demonstration of Work Done so far

Presentation schedule: 2nd – 7th November 2020
Platform for conducting presentations: Google Meet
Time per team: 20 Minutes

Note:

1. Guides will have to fill a Grading sheet (Shared Excel Sheet) giving marks out of 50 to their respective teams after the presentation.
   Link to the form: https://docs.google.com/spreadsheets/d/1U5bis9e1YHULZGyS1mtcziDxPIOqbkz3au8yVhxnHRk/edit?usp=sharing
2. Guides will have to save the recordings of the presentations conducted on google meet and share the link in a shared excel sheet of bimonthly report.

--
Regards
Prof. Mahendra Mehra
Assistant Professor,
Computer Engineering Department.
Fr.C.R.C.E
Bandra (West)
8149327826 / 7977664541

CEH Certified Ethical Hacker V8

STAFF_notice_mid term project ppt1 2020-21.pdf
579K

SAMPLE – FINAL YEAR PROJECT POSTER

eFSI

(E-Yantra Farm Setup Initiative, IIT Bombay)

Department of Computer Engineering,

Fr. Conceicao Rodrigues College of Engineering, *Bandra, Mumbai,*

Affiliated to Mumbai university

AIM

Initiative aims at setting up an automated agriculture project test bed to address real-world problems and hands-on learning for students to apply theory in a fun in a productive manner.

FLOW DIAGRAM

Preparing Trough

↓

Preparing Amrit Jal

↓

Preparing Amrit Mitti

↓

Preparing the Test Bed

↓

Sowing Seeds

↓

Setting up Automated Irrigation

Figure 1: Flow Diagram

Task 1: Preparing Through of HDPE

1. Cut the sheet of length 100cm .
2. Make four crease marks along its length & breadth at a distance of 20 cm each from the edges
3. Make four crease marks at corners at an angle of 45 degrees. Make two 8mm holes using a drill machine at a distance of 10 cm from center on either sides and at distance of 5cm from the edge of the sheet. Repeat this on the other side of the sheet
4. Fold the sheet along the crease marks to form a rectangular open box

Task 2: Preparing Amrit Jal

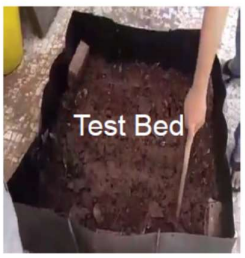
1. Organic Jaggry (100gm) + Cow Urine (1L) + Cow Dung (1 kg) + Water (10L) slurry is created
1. Stirring the slurry in clockwise direction (12 times), then in anti-clockwise direction (12 times)
2. Step 2 repeated slurry 3 times a day for the next 3 days
3. After 3 days Dilute 11 liters of slurry into 100 liters of water which will create 111 liters of Amrut Jal

Task 3: Preparing Amrit Mitti

1. Mix 20 kg biomass into Amrut Jal and keep it standing for 24 hrs.
2. 3 feet wide and 1 feet high from wet biomass Heap created
3. Heap was created using layers of Biomass, soil and rock-dust (incase soil is less pores)
4. The layer present are as follows
   - Layer 1 - Biomass
   - Layer 2: Soil
   - Repeat layer 1 & 2 up till layer 11
   - Layer 12: Rock dust
   - Apply pressure across heap every 10th layer of biomass.
   - Continue the above layering until you reach 1 feet

Task 4: Preparing Test Bed

1. Approximately 60 layers have been created
2. Heap is turned twice a week and Amrut Jal is sprayed to maintain moisture inside the heap
3. Every 7 days add Amrut Jal and water to keep the heap moist.
4. Turn the heap every 7 days for the next ONE month and add the Amrut Jal to keep the heap moist
5. One layer of soil-approximately 2 inches added before sowing of seed
6. After sowing top the seeds with mulch heap with biomass to protect the seeds from the birds

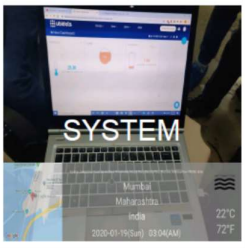


Task 5: Sowing Seeds

1. One layer of soil - approximately 2 inches is added
2. The seeds are Sown
3. Top the seeds with mulch heap with biomass to protect the seeds from birds.
4. Pruning of 25% leaves (21 Days after germination and then after 42 days)
5. Some plants may start flowering, cut all plants 0.5inch from soil and cut stem into 3-4 inch and keep it on heap for 3-4 days for drying (63 Days after germination)

Task 6 : Setting up automated irrigation

1. RaspPi Internet of things (IoT) Dashboard
2. Setting WIFI router ,Sensors , Light , Fan and Water Storage
3. Connecting all with RaspPi and supplying power to it
4. The sensors collect the data and send it to the cloud server with the help of Raspi and Hotspot
5. The sensors data is displayed with the help of an android app
6. The irrigation, light and fan are controlled by the Raspi based on the values from the sensors place inside the farm



SAMPLE – BE PROJECT ASSESSMENT

FEEDBACK FORM FORMAT FOR EXTERNAL

Fr.CRCE: BE Computer Major Project II External Examiner's Feedback

This is the Feedback form to be filled by External Examiner for project groups under Prof. Monali and Prof. Ashwini

* Required

1. Email address *

2. External Examiner Full Name *

3. External Examiner's College Name *

4. Contact No *

5. 1. Select the Project Evaluated *

Mark only one oval.

- ◯ Prof. Shetty Monali: Selection of optimal team based on players performance
- ◯ Prof. Shetty Monali: Virtual mouse using hand gesture
- ◯ Prof. Pansare Ashwini : RetinoDoc: A Diabetic Retinopathy Detection App
- ◯ Prof. Pansare Ashwini : Pothole detection using mobile sensor

6. PROJECT EVALUATION *

Mark only one oval per row.

	Excellent	Good	Average	Poor
Problem Statement	◯	◯	◯	◯
Literature Survey	◯	◯	◯	◯
Usage of Modern Tool/Technology	◯	◯	◯	◯
Design(s) and Implementation	◯	◯	◯	◯
Result Analysis	◯	◯	◯	◯
Oral Presentation and Project Demonstration	◯	◯	◯	◯
Overall Feedback on work done by the Project Team	◯	◯	◯	◯

7. Any other Comment (Optional)

8. 2. Select the Project Evaluated *

Mark only one oval.

- ◯ Prof. Shetty Monali: Selection of optimal team based on players performance
- ◯ Prof. Shetty Monali: Virtual mouse using hand gesture
- ◯ Prof. Pansare Ashwini : RetinoDoc: A Diabetic Retinopathy Detection App
- ◯ Prof. Pansare Ashwini : Pothole detection using mobile sensor

9. PROJECT EVALUATION *

Mark only one oval per row.

	Excellent	Good	Average	Poor
Problem Statement	◯	◯	◯	◯
Literature Survey	◯	◯	◯	◯
Usage of Modern Tool/Technology	◯	◯	◯	◯
Design(s) and Implementation	◯	◯	◯	◯
Result Analysis	◯	◯	◯	◯
Oral Presentation and Project Demonstration	◯	◯	◯	◯
Overall Feedback on work done by the Project Team	◯	◯	◯	◯

10. Any other Comment (Optional)

11. 3. Select the Project Evaluated *

Mark only one oval.

- ◯ Prof. Shetty Monali: Selection of optimal team based on players performance
- ◯ Prof. Shetty Monali: Virtual mouse using hand gesture
- ◯ Prof. Pansare Ashwini : RetinoDoc: A Diabetic Retinopathy Detection App
- ◯ Prof. Pansare Ashwini : Pothole detection using mobile sensor

12. PROJECT EVALUATION *

Mark only one oval per row.

	Excellent	Good	Average	Poor
Problem Statement	◯	◯	◯	◯
Literature Survey	◯	◯	◯	◯
Usage of Modern Tool/Technology	◯	◯	◯	◯
Design(s) and Implementation	◯	◯	◯	◯
Result Analysis	◯	◯	◯	◯
Oral Presentation and Project Demonstration	◯	◯	◯	◯
Overall Feedback on work done by the Project Team	◯	◯	◯	◯

13. Any other Comment (Optional)

14. 4. Select the Project Evaluated *

Mark only one oval.

- ◯ Prof. Shetty Monali: Selection of optimal team based on players performance
- ◯ Prof. Shetty Monali: Virtual mouse using hand gesture
- ◯ Prof. Pansare Ashwini : RetinoDoc: A Diabetic Retinopathy Detection App
- ◯ Prof. Pansare Ashwini : Pothole detection using mobile sensor

15. PROJECT EVALUATION *

Mark only one oval per row.

	Excellent	Good	Average	Poor
Problem Statement	◯	◯	◯	◯
Literature Survey	◯	◯	◯	◯
Usage of Modern Tool/Technology	◯	◯	◯	◯
Design(s) and Implementation	◯	◯	◯	◯
Result Analysis	◯	◯	◯	◯
Oral Presentation and Project Demonstration	◯	◯	◯	◯
Overall Feedback on work done by the Project Team	◯	◯	◯	◯

16. Any other Comment (Optional)

Examiners NEFT DETAILS

Please provide your NEFT details

17. Account Holder Name *

18. Account No *

19. IFSC CODE *

20. BANK NAME *

21. BRANCH ADDRESS *

SAMPLE – UNIT TEST QUESTION PAPER

Fr. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING.
Unit Test-II

SEMESTER / BRANCH: **VII/ COMPUTER**
SUBJECT: **Big Data Analytics** MAX. MARKS: 20
DATE: **16/10/2019** TIME: 11.30AM-12.30PM

CSDLO7032.4: Interpret business models and scientific computing paradigms, and apply software tools for big data analytics. [B3: Application]
CSDLO7032.5: Adapt adequate perspectives of big data analytics in various applications like Recommender systems, Social Media applications etc. [B3: Application]

Q. 1. Identify the algorithm and show the working **(any three)** ***[CO4] (15 Marks)***

a) The sensor generates the continuous stream of data about temperature. If the temperature at any instant is above certain average temperature then that is represented as 1 otherwise 0. Count how many times the sensor reading was above the average temperature (number of ones) in the data stream in last k readings (bits) (k=20) using appropriate algorithm. **10110101011011** Then if the new bits **10111** arrive; Show change in the states of the buckets. Compare the Estimated answer with Actual answer and comment. What is the complexity of the applied algorithm?

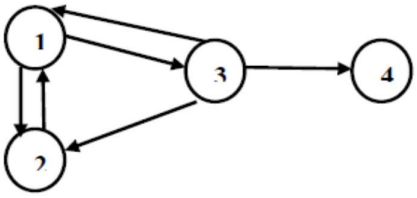
b) The University has the data set of all the professor profiles and their salary. All the data points are not normally distributed across the centroid. Identify the suitable algorithm for clustering such a big data set and explain its working with analysis.

c) There are three web pages indicated as nodes n1 to n3. The random surfer may visit the pages using hyperlinks. This is represented using the adjacency matrix for a graph.

$$A = \begin{matrix} 1 & 1 & 1 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{matrix}$$

Calculate the authority and hub scores for this graph using the suitable algorithm with **k=2** and Identify the best authority and hub nodes.

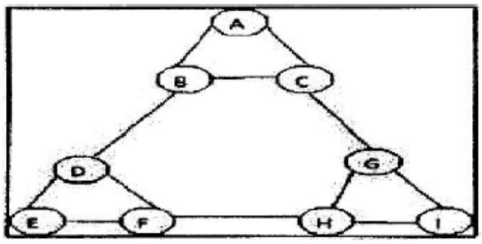
d) Compute the page rank of nodes (refer Fig Q1-d) with teleport factor 0.8. (Show two iterations). Does this network have dead ends and spider traps?



Q. 2. Answer **any one** question. ***[CO5](05 Marks)***

a) Define content based recommendation systems. Using an example case study describe how it can be used to provide recommendations to users.

b) The whaps-app network is shown in the graph (Refer fig Q2-b). Find all **two level** communities using a suitable algorithm using the edge betweenness factor.



SAMPLE – STUDENT REPORT CARD INTERNAL ASSESSMENT

Fr. Conceicao Rodrigues College of Engineering

Fr Agnel Ashram, Bandstand, Bandra (W), Mumbai - 400050
URL: www.fragnel.edu.in Ph: +912267114168 Mail: exam@fragnel.edu.in

STUDENT PERFORMANCE REPORT

Dear Parent,

Subject: ***Performance report of Mr. / Ms. Gupta Hrithik Anil***

Please find the performance report of your ward Gupta Hrithik Anil [Roll. No. 8542] after the 9 Weeks of classes and Internal assessment test - 1. We would like to inform you that minimum of 75 % overall attendance is required to become eligible for the Term End University Examination. Term End examination is expected to begin from third week of Nov, 2019. Internal assessment test(s) are separate passing heads and failure in the IA Test indicates failure in the Term End University examination. We request you to kindly help us in improving the student's performance by taking necessary steps possible from your end. This would strengthen our efforts in this regard.

We request you to get in touch with the Electronics Engineering Class teacher Prof. Heenakausar Pendhari to discuss & understand the performance of your ward.

Prof. Heenakausar Pendhari may be reached on Phone: +91-022- and e-Mail: heenak.pendhari@fragnel.edu.in

Attendance Report

Subject Name	Type	CC	AC	%Atten
Applied Mathematics - III	TH	25	12	48%
Digital Circuit Design	TH	29	14	49%
Electronics Instruments & Measurement	TH	18	8	45%
Electrical Network & Measurement Lab.	PR	5	3	60%
Electronic Devices & Circuits I Lab.	PR	5	2	40%
Applied Mathematics - III	TU	3	3	100%

Subject Name	Type	CC	AC	%Atten
Electronic Devices & Circuits I	TH	28	15	54%
Electrical Network Analysis & Synthesis	TH	28	24	86%
Object Oriented Prog. Methodology Lab.	TH	13	8	62%
Digital Circuit Design Lab.	PR	5	4	80%
Object Oriented Prog. Methodology Lab.	PR	5	4	80%

TH: Theory PR: Practical TU: Tutorial CC: Conducted Classess / Sessions AC: Attended Classess / Sessions NA: Not Applicable

Overall % attendance: 60 %

Internal Assessment Test Marks Report

Subject Name	Type	Max Marks	Secured Marks	% Marks / Result
Applied Mathematics - III	TH	20	2	10% / Fail
Electronic Devices & Circuits I	TH	20	14	70% / Pass
Digital Circuit Design	TH	20	6	30% / Fail
Electrical Network Analysis & Synthesis	TH	20	-- NA -- 00	fail
Electronics Instruments & Measurement	TH	20	4	20% / Fail
Object Oriented Prog. Methodology Lab.	TH	0	0	0% / Fail

TH: Theory NA: Not Applicable

Parent's Remarks & Signature	DeepJaxmi

Principal
DR. (MRS.) SRIJA UNNIKRISHNAN
PRINCIPAL

Head of Department

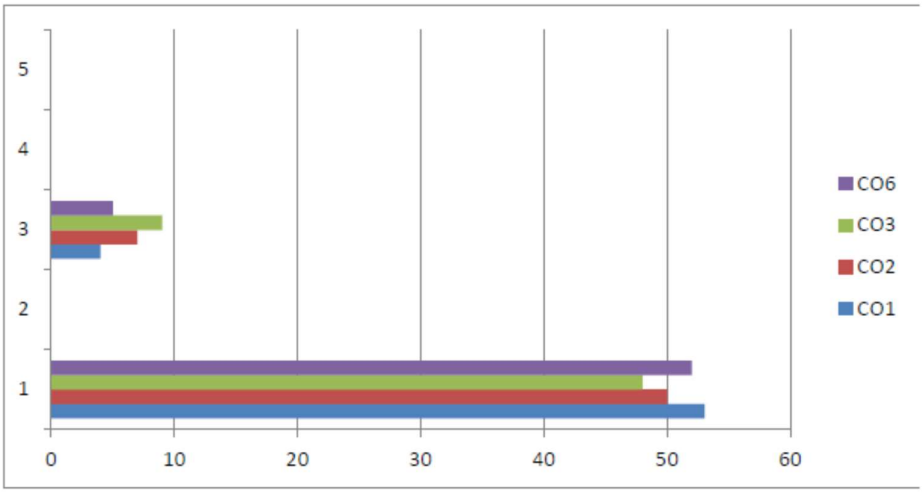
29/08/19
Class Teacher

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
FR. AGNEL ASHRAM, BANDRA (W) MUMBAI-50

Do not Print this document unless it is very necessary. Save Environment. Save Trees. e-Governace initiative - Fr. CRCE

SAMPLE – COURSE EXIT SURVEY

FR.C.R.C.E Department of Computer Engineering							
Subject: Big Data Analytics (CSDLO7032) Year: 2019-2020							
Course Exit Survey							
Rating	5	4	3	2	1		
CO1	53		4				
CO2	50		7				
CO3	48		9				
CO4	50		7				
CO5	51		6				
CO6	52		5				



SAMPLE – MID TERM FEEDBACK

FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering
2019-2020
Mid Term Feedback Report

To enhance the quality of teaching/learning process, midterm feedback was conducted across all the semesters' on19th August 2019 (Odd) & 28th February 2020- (Even). This was in addition to college level student's feedback. Following question were asked to students,

A) Subject wise teaching Learning feedback

Knowledge of the teacher on the subject
Clarity and understandability of teacher's explanation9 responses
Effectively used lecture time
Ability to hold attention
Speed of Presentation
Ability to encourage interaction
Accessibility outside the class
Engagement of all lectures according to time table on regular basis
Ability to be unbiased
Overall Teaching effectiveness of the teacher
Any Additional Information

B) Facilities/ activities

Lab facility
Internet/Wifi Facilities
Library Facilities
Sports and cultural facilities and actives
Students counseling, mentoring and Guidance

C) Curriculum aspects, Carrier Guidance and overall development

Seminars and workshops related with recent technological development
Guidance for Placement, Higher studies and Entrepreneurship
Any specific remark on overall development

General Observation

- Overall students were happy with the teaching/learning method.
- Lab facilities were observed well except for Internet speed and more Wi-Fi access points.
- Library facilities were fairly good
- Proper guide lines on project based learning
- Requested weightage in academic for house Internship
- Smart classrooms for effective teaching learning process

- Requested for industry internships and higher studies guidance, competitive programming
- Project Lab with facilities on machine learning

Subject wise feedback was communicated to the respective teacher to improve the process.

(Dr. B. S. Daga)
HoD ,Computer Engineering